AN3961
Application note

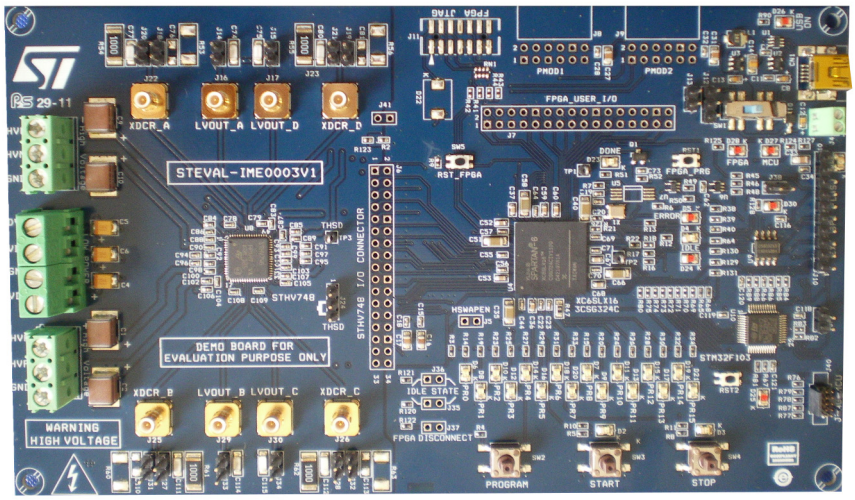
STEVAL-IME003V1 demonstration board based on the STHV748 high voltage pulser

Introduction

The STEVAL-IME003V1 demonstration board is designed around the STHV748 4-channel high voltage pulser, a state-of-the-art device designed for ultrasound imaging applications.

The output waveforms can be displayed directly on an oscilloscope by connecting the scope probe to the relative BNCs. 16 preset waveforms are available to test the HV pulser under varying conditions.

Figure 1. Photo of the STEVAL-IME003V1



Warning: **Beware before applying any voltage supply to the STEVAL-IME003V1 please read carefully the instructions contained in this document.**

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1 Board features

- Based on the STHV748 device for ultrasound imagine applications
- 4 monolithic channels, 5 level high voltage pulser
- Integrated T/R switch
- On-board equivalent piezoelectric load implemented by means of:
  - R/C equivalent network
  - SMD landing areas available for a customized output load
- USB interface available to upload customized output waveforms
- 4 Mb serial Flash memory available for storing customized waveforms
- Memory expansion connector is available to expand serial Flash size
- High voltage and low voltage connectors to power the STHV748
- 25 LEDs to check the board status and proper operation
- Human machine interface to select, start and stop the stored output waveforms

2 Getting started

To use the STEVAL-IME003V1, perform the following steps:

1. Connect the power supply to the board (see *Section 3.1*)
2. Connect the BNC to the oscilloscope.
3. Check that switch SW1 is set to the FPGA position.
4. Check that the LED indicator DONE (D23) turns on.
5. Check that FPGA is in the idle state (LED D4 is on)
6. Select the waveform with the PROGRAM button. The corresponding program LED (D6-D29) turns on.
7. Press the START button to run the selected program; the START LED (D2) turns on. After program ends, the FPGA returns to the idle state (LED D4 is on).
8. If a continuous wave program has been selected (Program “2”), the button STOP must be pressed to stop program execution. The FPGA returns to the idle state and the STOP LED (D3) turns on.
9. To run the same program again, restart from step 7. To run a different program, restart from step 6.

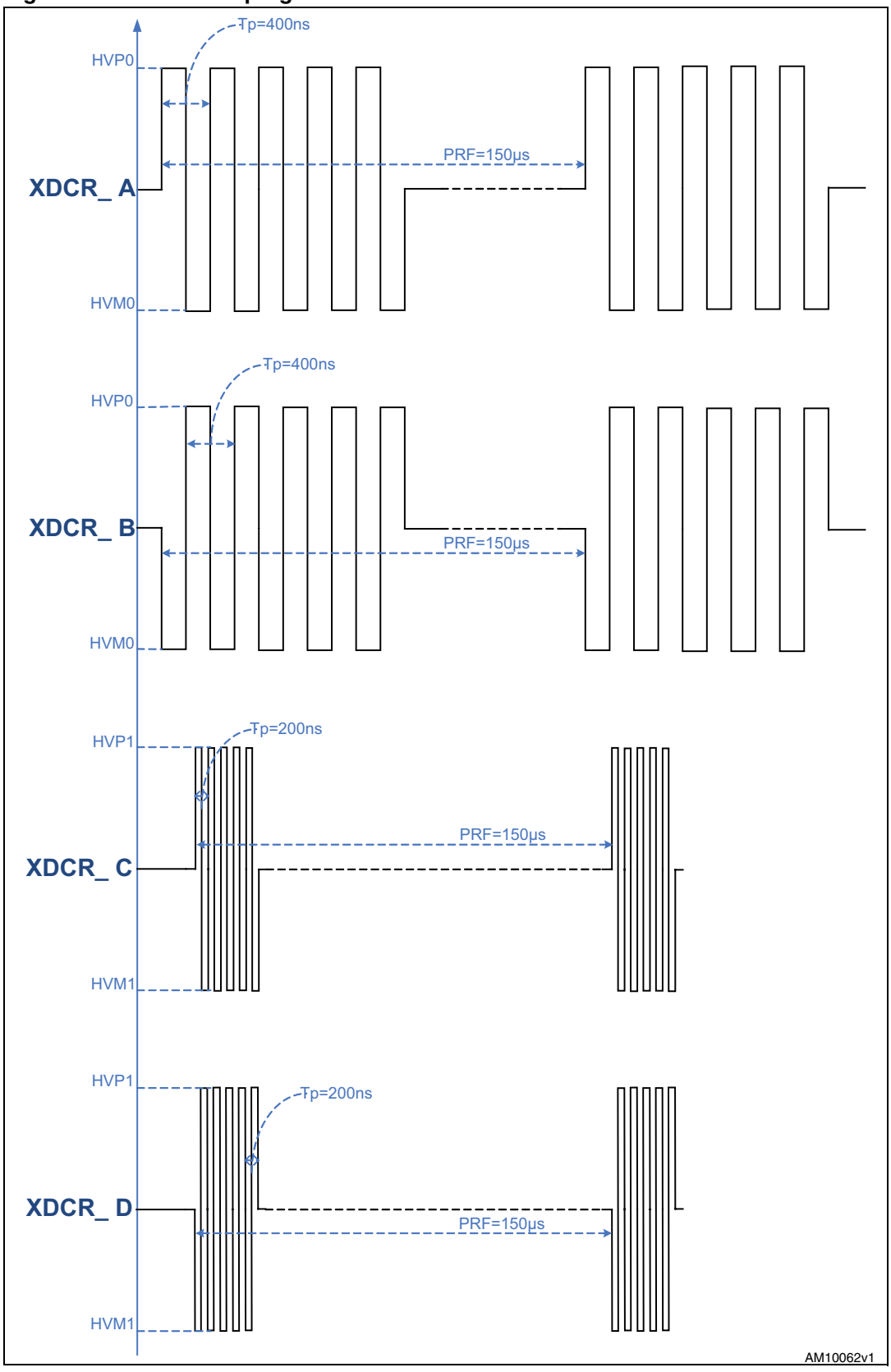
2.1 Programming waveform description, flagged by LED (D6-D9)

Program “0” (see *Figure 2*)

- XDCR_A: pulse wave mode, TX0 switching, 5 pulses, time-period T_P=400 ns and PRF=150 µs
- XDCR_B: pulse wave mode, TX0 switching, 5 pulses in counter phase respect to XDCR_A, time-period T_P=400 ns and PRF=150 µs
- XDCR_C: pulse wave mode, TX1 switching, 5 pulses, time-period T_P=200 ns and PRF=150 µs
- XDCR_D: pulse wave mode, TX1 switching, 5 pulses in counter phase respect to XDCR_C, time-period T_P=200 ns and PRF=150 µs

Note: TX0 means H-bridge supplied by HVP/M0, while TX1 means H-bridge supplied by HVP/M1.

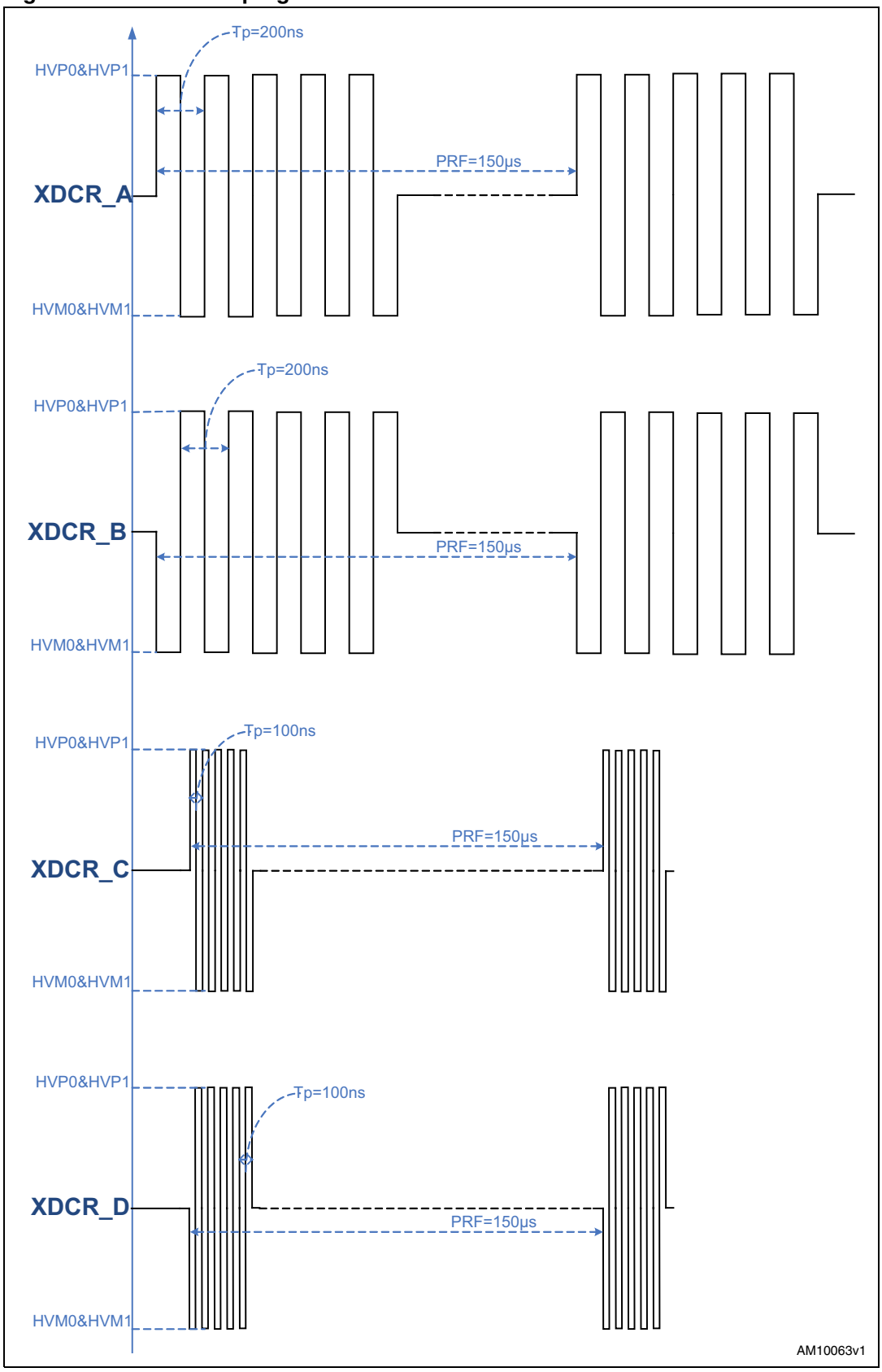
Figure 2. Scheme of program “0”



Program “1” (see *Figure 3*)

- XDCR_A: pulse wave mode, TX0&TX1 (half-bridges in parallel) switching, 5 pulses, time-period TP=200 ns and PRF=150 µs.
- XDCR_B: pulse wave mode, TX0&TX1 (half-bridges in parallel) switching, 5 pulses in counter phase respect to XDCR_A, time-period T_P=200 ns and PRF=150 µs.
- XDCR_C: pulse wave mode, TX0&TX1 (half-bridges in parallel) switching, 5 pulses, time-period TP=100 ns and PRF=150 µs.
- XDCR_D: pulse wave mode, TX0&TX1 (half-bridges in parallel) switching, 5 pulses in counter phase respect to XDCR_C, time-period T_P=100 ns and PRF=150 µs.

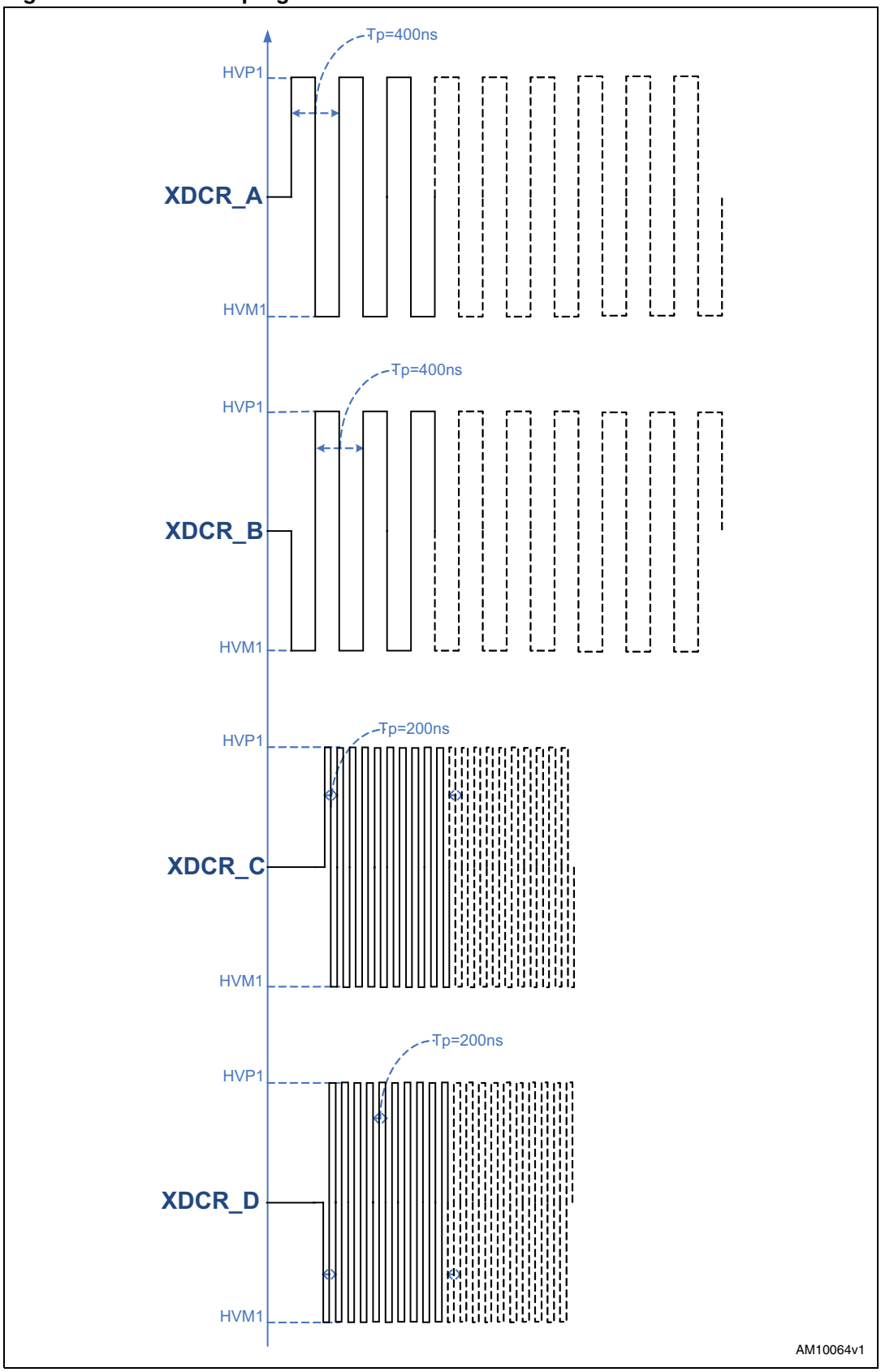
Figure 3. Scheme of program “1”



Program “2” (see *Figure 4*)

- XDCR_A: continuous wave mode, TX-CW switching, time-period T_P=400 ns.
- XDCR_B: continuous wave mode, TX-CW switching in counter-phase respect to XDCR_A, time-period T_P=400 ns.
- XDCR_C: continuous wave mode, TX-CW switching, time-period T_P=200 ns.
- XDCR_D: continuous wave mode, TX-CW switching in counter-phase respect to XDCR_C, time-period T_P=200 ns.

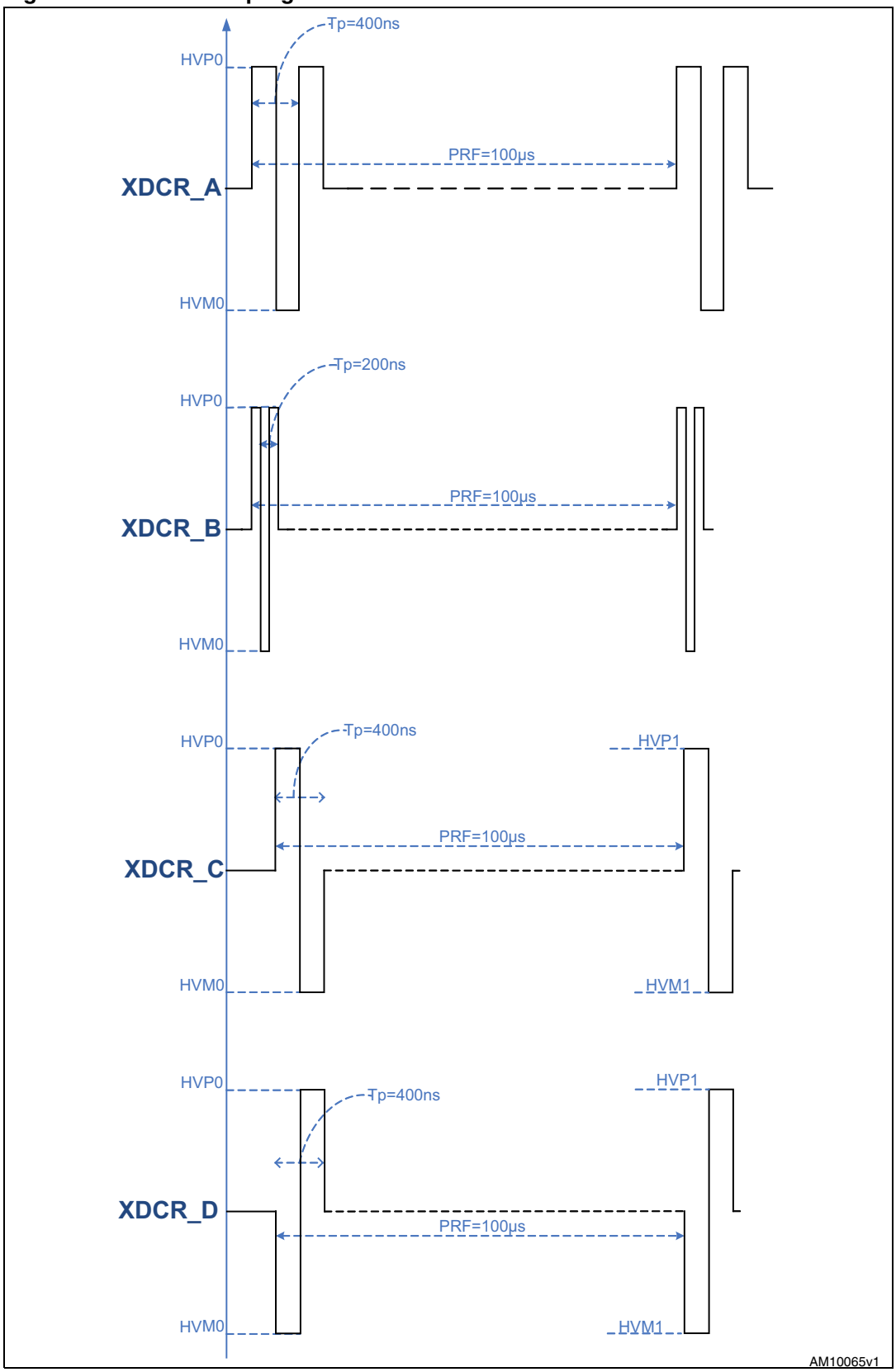
Figure 4. Scheme of program “2”



Program “3” (see *Figure 5*)

- XDCR_A: pulse wave mode, TX0 switching, 1.5 pulses, time-period T_P=400 ns and PRF=100 µs.
- XDCR_B: pulse Wave mode, TX0 switching, 1.5 pulses, time-period T_P=200 ns and PRF=100 µs.
- XDCR_C: pulse wave mode, TX0 switching 1pulses and consequently TX1 switching 1pulses, time-period T_P=400 ns and PRF=100 µs.
- XDCR_D: pulse wave mode, TX0 switching 1pulses and consequently TX1 switching 1pulses both in counter phase respect to XDCR_C, time-period T_P=400 ns and PRF=100 µs.

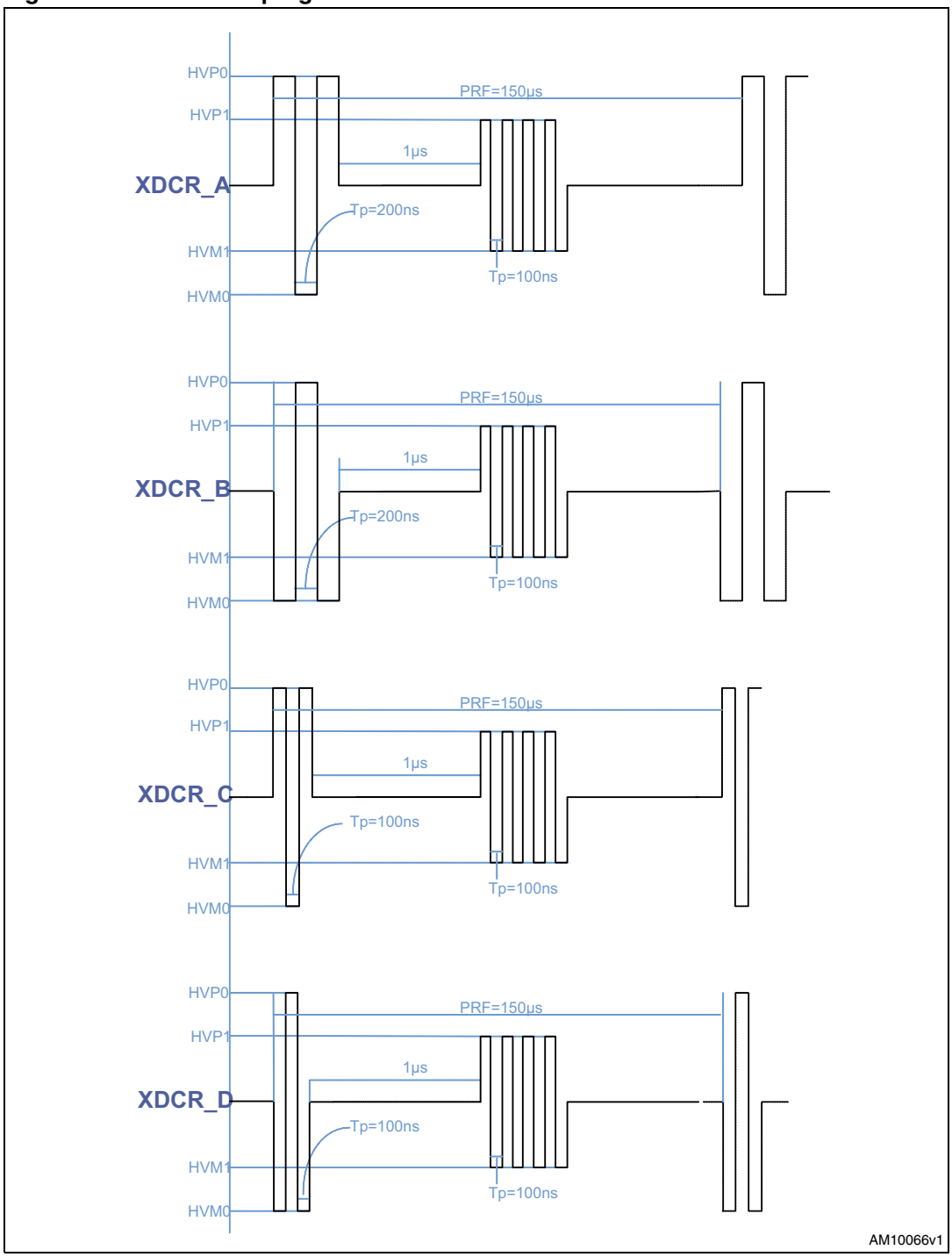
Figure 5. Scheme of program “3”



Program “4” (see *Figure 6*)

- XDCR_A: 5 level mode example, STATE sequence; clamp-->HVP0-->HVM0-->HVP0-->clamp (1 µs)-->HVP1-->HVM1-->HVP1-->HVM1-->HVP1-->HVM1-->HVP1-->HVM1-->clamp, Tp=200 ns and PRF=150 µs.
- XDCR_B: 5 level mode example, STATE sequence; clamp-->HVM0-->HVP0-->HVM0-->clamp (1 µs)-->HVP1-->HVM1-->HVP1-->HVM1-->HVP1-->HVM1-->HVP1-->HVM1-->clamp, Tp=200 ns and PRF=150 µs.
- XDCR_C: 5 level mode example, STATE sequence; clamp-->HVP0-->HVM0-->HVP0-->clamp (1 µs)-->HVP1-->HVM1-->HVP1-->HVM1-->HVP1-->HVM1-->HVP1-->HVM1-->clamp, Tp=100 ns and PRF=150 µs.
- XDCR_D: 5 level mode example, STATE sequence; clamp-->HVM0-->HVP0-->HVM0-->clamp (1 µs)-->HVP1-->HVM1-->HVP1-->HVM1-->HVP1-->HVM1-->HVP1-->HVM1-->clamp, Tp=100 ns and PRF=150 µs.

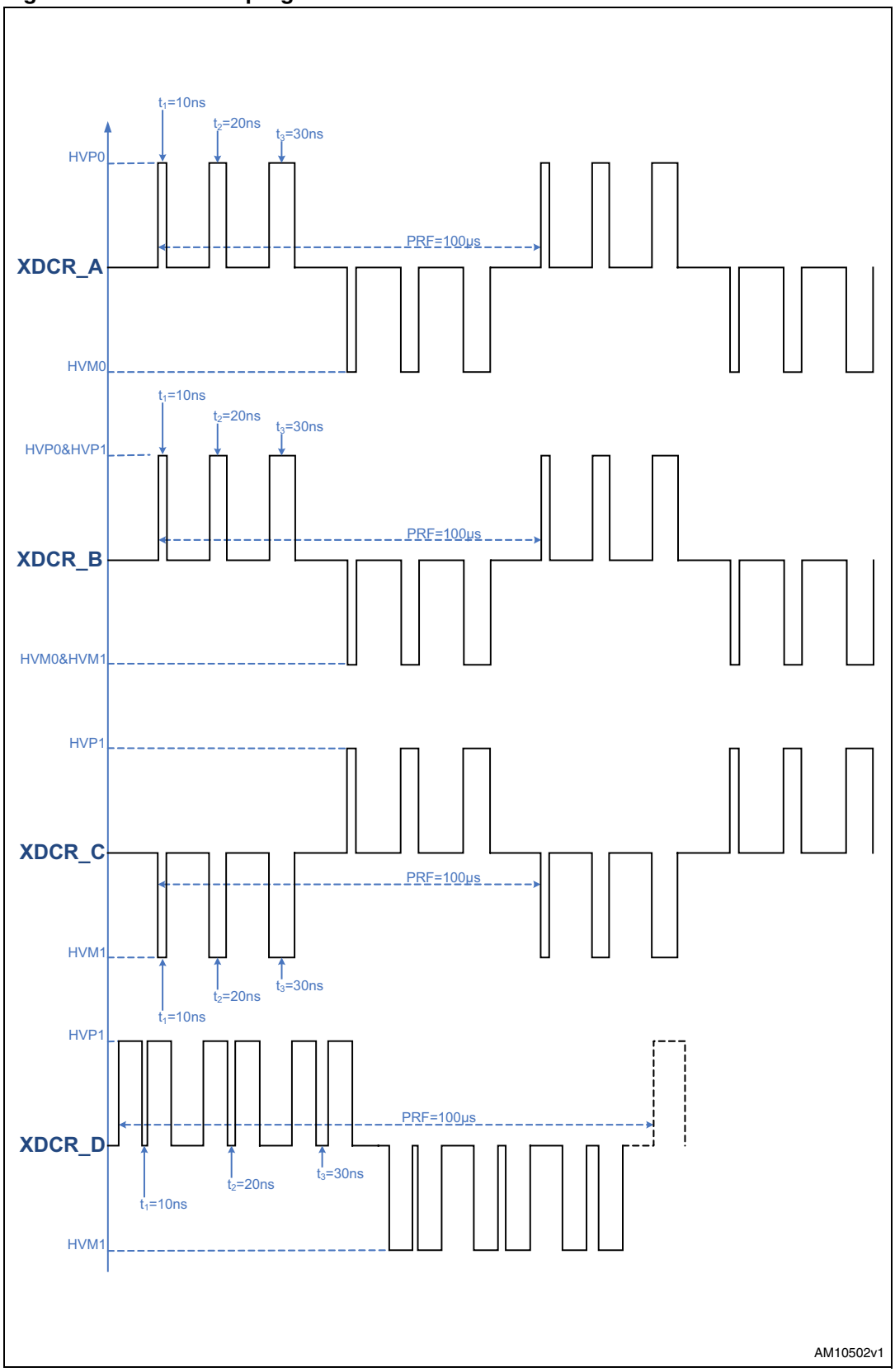
Figure 6. Scheme of program “4”



Program “5” (see *Figure 7*)

- XDCR_A: Short pulses mode example, STATE sequence; TX0 switching, Clamp --> HVP0 (10 ns) --> Clamp --> HVP0 (20ns) --> Clamp --> HVP0 (30 ns) --> Clamp --> HVM0 (10 ns) --> Clamp -->HVM0 (20 ns) --> Clamp -->HVM0 (30 ns) -->Clamp, PRF=150 µs.
- XDCR_B: Short pulses mode example, STATE sequence; TX0//TX1 switching, Clamp --> HVP0&1 (10 ns) --> Clamp --> HVP0&1 (20 ns) --> Clamp --> HVP0&1 (30 ns) --> Clamp --> HVM0&1 (10 ns) --> Clamp -->HVM0&1 (20 ns) --> Clamp -->HVM0&1 (30 ns) -->Clamp, PRF=150 µs.
- XDCR_C: Short pulses mode example, STATE sequence; TX1 switching, Clamp --> HVM0 (10 ns) --> Clamp --> HVM1 (20 ns) --> Clamp --> HVM1 (30 ns) --> Clamp --> HVP1 (10 ns) --> Clamp -->HVP1 (20 ns) --> Clamp -->HVP1 (30 ns) -->Clamp, PRF=150 µs.
- XDCR_D: Short clamp mode example, STATE sequence; TX1 switching, Clamp --> HVP1 --> Clamp (10 ns) --> HVP1 --> Clamp --> HVP1 --> Clamp (20 ns) --> HVP1 --> Clamp --> HVP1 --> Clamp (30 ns) --> HVP1 -->clamp--> HVM1 --> Clamp (10 ns) --> HVM1 --> clamp -->HVM1 --> Clamp (20 ns) --> HVM1 --> Clamp --> HVM1 -->Clamp (30 ns) --> HVM1--> Clamp.

Figure 7. Scheme of program “5”



3 Hardware layout and configuration

The STEVAL-IME003V1 demonstration board is designed around the STHV748. The hardware block diagram (*Figure 8*) illustrates the main connection between the STHV748, the FPGA, the STM32F103C8T6 and the SPI Flash memory. *Figure 9* shows the location of the connectors, LEDs and features on the board.

Figure 8. Hardware block diagram

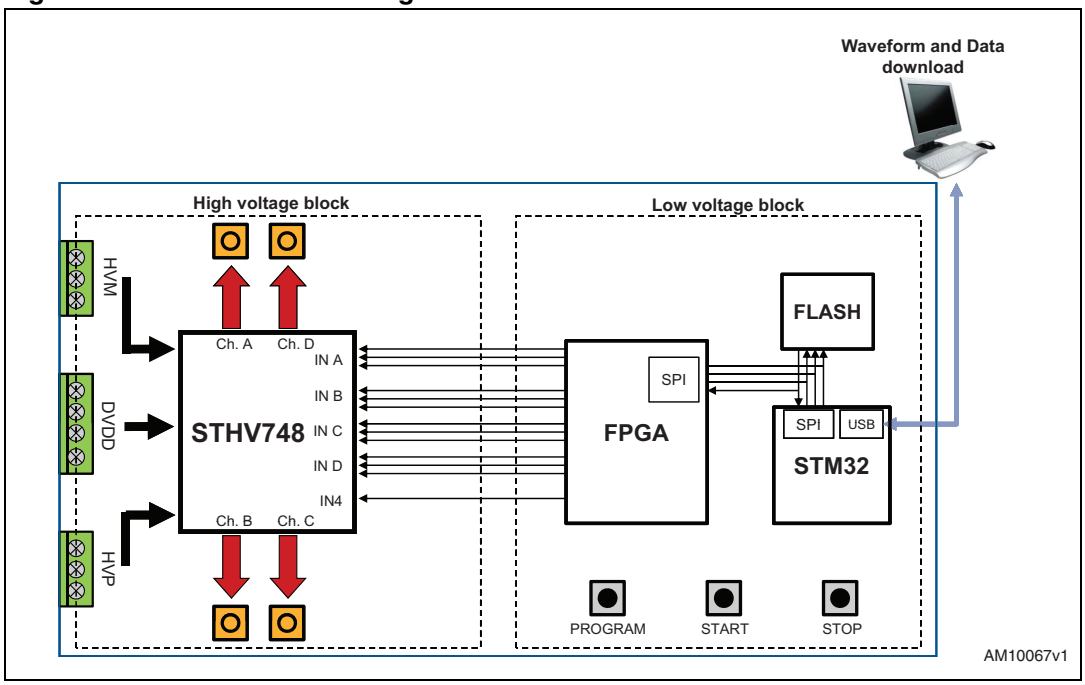
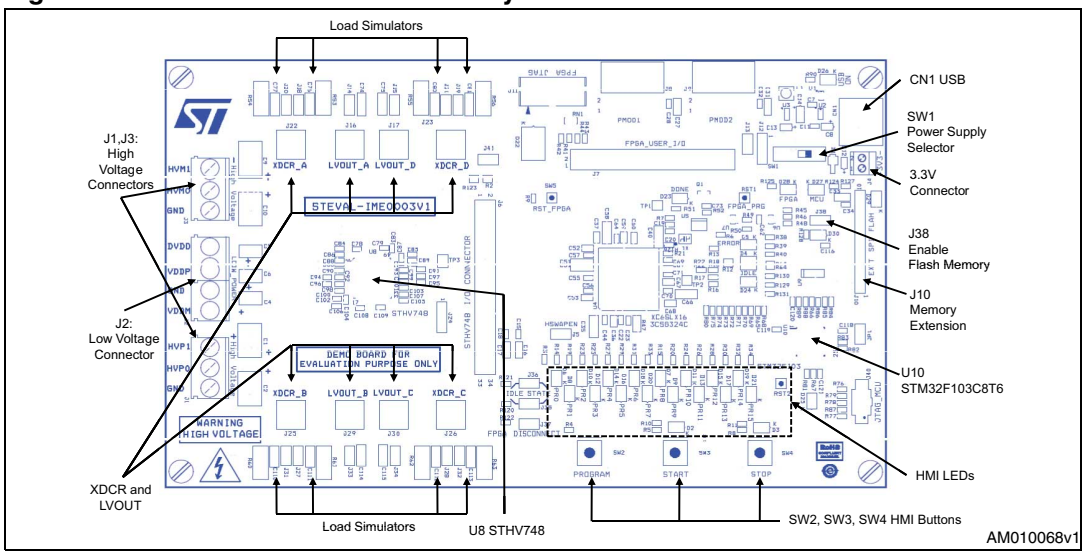


Figure 9. STEVAL-IME003V1 board layout



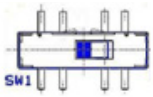
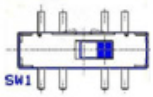
3.1 Power supply

The low voltage block of the STEVAL-IME003V1 board is designed to be powered by:

- 3.3 V DC connected to J4 to supply FPGA and SPI Flash memory
- 5 V DC through USB Mini B connector to supply the STM32 and the SPI memory

The power supply is configured by setting SW1 and J41 as described in *Table 1*.

Table 1. Power related jumpers

	Description	
SW1		For normal operation mode, to supply FPGA and SPI Flash memory (default setting)
		For update operation mode, to supply STM32F103 and SPI Flash memory
J41	FPGA and SPI Flash memory are supplied by DVDD (J2). (Not mounted on PCB)	

Note: The fitting of J41 can create a voltage mismatch between J4 and J2 when one of these is not 3.3 V.

LED D26, D27 and D28 show the power supply configuration as described in *Table 2*.

Table 2. Power supply LED

	Color	Name	Description
D26	Red	USB ON	The USB cable is connected
D27	Red	MCU	Update operation mode, to supply power to STM32F103 and SPI Flash memory
D28	Red	FPGA	Normal operation mode, to supply power to FPGA and SPI Flash memory.

The high voltage block of the STEVAL-IME003V1 is designed to be powered by the following (see *Table 15* for maximum rating):

- DVDD: logic voltage, 0 to 3 V (J2 conn.)
- VDDP: positive supply voltage 0 to 3 V (J2 conn.)
- VDDM: negative supply voltage -3 V to 0 (J2 conn.)
- GND: ground (J2 conn.)
- HVM0: TX0 high voltage negative supply (J3 conn.)
- HVM1:TX1 high voltage negative supply (J3 conn.)
- GND: ground (J2 conn.)
- HVP0:TX0 High voltage positive supply (J1 conn.)
- HVP1:TX1 High voltage positive supply (J1 conn.)
- GND: ground (J1 conn.)

It is recommended to follow a precise Power Up sequence, it depends on how many level the user would have.

3-levels, switch on:

1. 3.3 V on J4
2. VDDP and DVDD on J2
3. VDDM on J2
4. HVM0 and HVM1 on J3
5. HVP0 and HVM1 on J1

5-levels, switch ON:

1. 3.3 V on J4
2. VDDP and DVDD on J2
3. VDDM on J2
4. HVM0 on J3
5. HVP0 on J1
6. HVM1 on J3
7. HVP1 on J1

The same care has to be respected for the power down sequence. It is reverse to the power up.

3-levels, switch off:

1. HVP0 and HVM1 on J1
2. HVM0 and HVM1 on J3
3. VDDM on J2
4. VDDP and DVDD on J2
5. 3.3 V on J4

5-levels, switch on:

1. HVP1 on J1
2. HVM1 on J3
3. HVP0 on J1
4. HVM0 on J3
5. VDDM on J2
6. VDDP and DVDD on J2
7. 3.3 V on J4

3.2 MCU

The STM32F103C8T6 is dedicated to updating the waveform and the FPGA bitstream on the SPI Flash memory. It is already pre-programmed as a DFU (device firmware upgrade) device, it has the ability to upgrade internal and external Flash memory. The STM32F103 manages all the DFU operations, such as the authentication of the product identifier, vendor identifier, firmware version and the alternate setting number (Target ID). It is used to upgrade the SPI Flash memory hosted on the STEVAL-IME003V1, and makes the upgrade more secure.

Note: See UM1083 for further details about the upgrade through DFU.

3.3 SPI Flash memory

The STEVAL-IME003V1 hosts a Micron N25Q032 (U9), which is a 32 Mbit (4 Mb x 8) serial Flash memory with advanced write protection mechanisms. It can be accessed through a high speed SPI-compatible bus and provides the possibility to work in XIP (“eXecution in Place”) mode.

The N25Q032 also supports high-performance quad I/O instructions. These instructions allow to quadruple the transfer bandwidth for read and program, and it is used by the FPGA.

If the 4 Mbyte memory it is not enough to contain the data, the user can connect an external Flash memory to the J10 connector. When the external Flash is connected, LED D29 is on (*Table 3*)

Table 3. SPI Flash memory LED

	Color	Name	Description
D29	Green	EXT SPI-FLASH	The external SPI-Flash module is connected

The Flash memory is configured by setting J38 as described in *Table 4*.

Table 4. SPI Flash memory jumper

	Description
J38	J38 should be fitted to power supply the on board SPI Flash memory. Default setting: Fitted.

3.4 FPGA

The STEVAL-IME003V1 includes a Xilinx Spartan®-6 XC6SLX16 FPGA which drives the STHV7478 pulser by generating a suitable sequence of digital control signals (called “program”). The board can store 16 programs which can be individually selected. The main features of waveforms generated by a program are summarized in *Table 5*.

Table 5. Program waveforms main features

Feature	Min	Typ.	Max
Waveform number	-	13	-
Time resolution	-	5 ns	-
Duration	40 ns	-	20.48 µs
Cycles number	1	-	255
Infinite cycle	Defined by the program		

Data required to generate a program are stored in the SPI Flash memory. When the program starts, data are downloaded from Flash memory and stored in FPGA internal RAM blocks. Then data is managed in order to generate the high-speed STHV748 digital control signals.

The SPI Flash also contains the FPGA configuration data (“bit stream”) which are automatically loaded during startup and after the FPGA reset (SW5) is pressed.

The FPGA is configured by setting jumpers as described in *Table 6*.

Table 6. FPGA jumpers

	Description
J5	J5 is used to control FPGA I/O pull-ups during configuration. It should be fitted to enable I/O pull-ups during FPGA configuration. Default setting: not mounted.
J12	Force FPGA into suspend mode
	Allow the STM32 to control FPGA suspend mode (default setting)
J13	J13 is used to prevent FPGA programming from configuration source. Fitted: disable FPGA programming. Unfitted: enable FPGA programming. (default setting: unfitted)
J35 and J36	Configure J35 and J36 to set up the outputs idle state as follows: (default setting: not mounted)
	High Z
	Clamp / HVR_SW
	High Z
	Clamp
J37	Configure J37 to connect FPGA outputs to STHV748 (default setting: not mounted)
	Fitted: disconnect FPGA outputs (high Z)
	Unfitted: connect FPGA outputs

The LEDs associated with FPGA operations are described in *Table 7*.

Table 7. FPGA LED

	Color	Name	Description
D2	Green	START	A program is running after START button SW5 has been pressed.
D3	Green	STOP	The STOP button SW4 has been pressed.
D4	Green	IDLE	The FPGA state machine is in the idle state.
D5	Red	ERROR	An error has occurred during FPGA state machine execution.
D23	Green	DONE	The FPGA has been successfully configured.
D6-D29	Yellow	PROG 0-15	The corresponding program is selected

3.4.1 Stored patterns

The STEVAL-IME003V1 offers the possibility to memorize 16 patterns into on-board Flash memory in order to show the performance achievable at the pulser outputs. Six selectable patterns already stored in the Flash memory are preset by default, available and ready to use. A detailed description of the preset programs is listed in the tables that follow.

Table 8. Program “0“

PW 5pulses - HV0/1=±60 V; load: 300 pF//100 Ω						
	mode	**Frequency [MHz]**	**Number of pulses**	**Initial pulse**	**H-bridge**	**PRF**
Ch A	PW	2.5	5	Positive	TX0	150 µs
Ch B	PW	2.5	5	Negative	TX0	150 µs
Ch C	PW	5	5	Positive	TX1	150 µs
CH D	PW	5	5	Negative	TX1	150 µs

Figure 10. Acquisition by program “0”

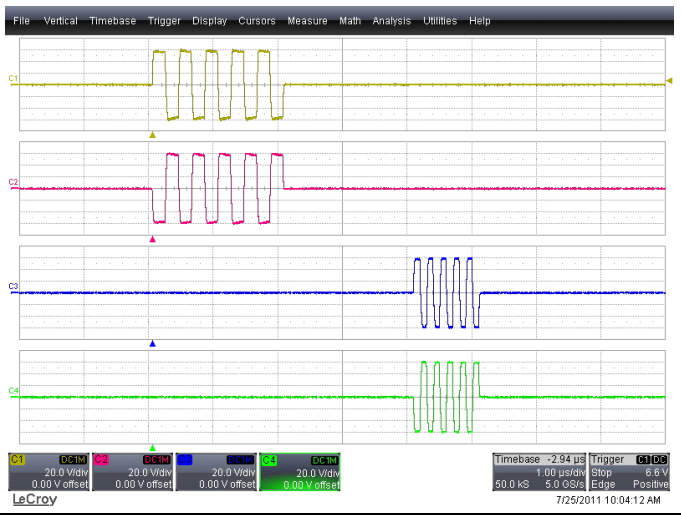


Table 9. Program “1”

PW TX0 and TX1 5pulses - HV0/1=±60 V; Load: 300 pF//100 Ω						
	mode	**Frequency [MHz]**	**Number of pulses**	**Initial pulse**	**H-bridge**	**PRF**
Ch A	PW	5	5	Positive	TX0 & TX1	150 µs
Ch B	PW	5	5	Negative	TX0 & TX1	150 µs
Ch C	PW	10	5	Positive	TX0 & TX1	150 µs
CH D	PW	10	5	Negative	TX0 & TX1	150 µs

Figure 11. Acquisition by program “1”

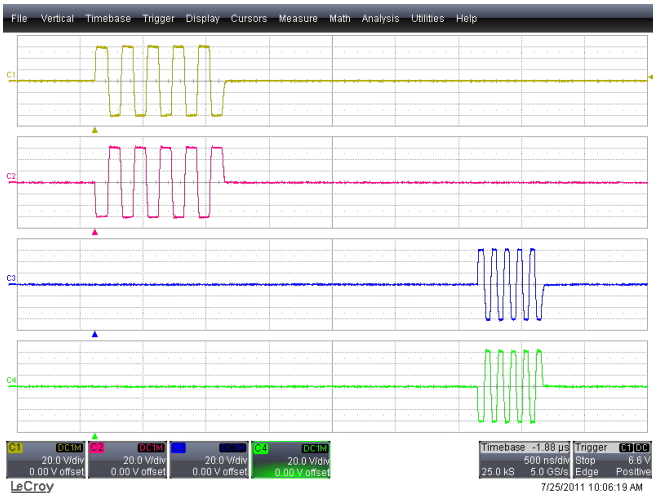


Table 10. Program “2”

Continuous wave - HV1=±10 V; load: 300 pF//100 Ω					
	mode	**Frequency [MHz]**	**Number of pulses**	**Initial pulse**	**H-bridge**
Ch A	CW	2.5	Continuous wave	Positive	TX-CW
Ch B	CW	2.5	Continuous wave	Negative	TX-CW
Ch C	CW	5	Continuous wave	Positive	TX-CW
CH D	CW	5	Continuous wave	Negative	TX-CW

Figure 12. Acquisition by program “2”

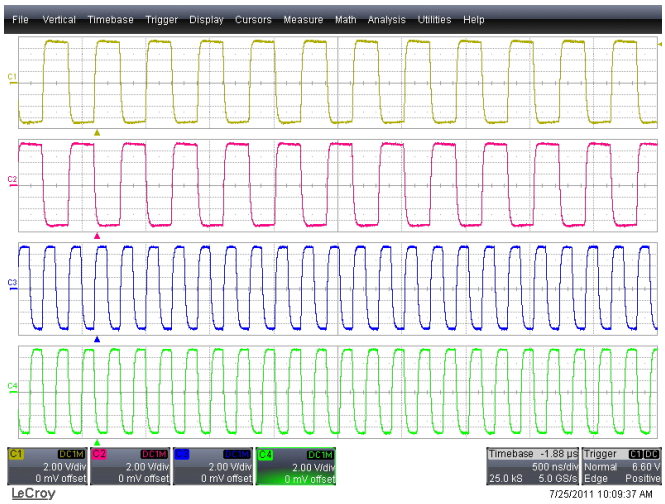


Table 11. Program “3”

Pulse cancellation - HV0/1=±60 V; load: 300 pF//100 Ω						
	mode	**Frequency [MHz]**	**Number of pulses**	**Initial pulse**	**H-bridge**	**PRF**
ChA	PC	2.5	3 half pulse		TX0	100 µs
ChB	PC	5	3 half pulse		TX0	100 µs
ChC	PC	2.5	2 half pulse	Positive	1 pul TX0 and 1pul TX1	100 µs
ChD	PC	2.5	2 half pulse	Negative	1 pul TX0 and 1pul TX1	100 µs

Figure 13. Acquisition by program “3”

File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help
C1
C2
C3
C4
C1 DC1M 20.0 V/div 0.00 V offset
C2 DC1M 20.0 V/div 0.00 V offset
C3 DC1M 20.0 V/div 0.00 V offset
C4 DC1M 20.0 V/div 0.00 V offset
Timebase -2.32 µs 500 ns/div 25.0 kS 5.0 GS/s
Trigger C1 DC Stop 6.6 V Edge Positive
LeCroy
7/25/2011 10:12:07 AM

Table 12. Program “4”

Five level - HV1=±40 V, HV0=±80 V; Load: 300 pF//100 Ω					
	Mode	**Time width per level**	**Number of pulses**	**Initial pulse**	**PRF**
ChA	5 level	1.5 cycle, 200 ns per level @ ±80 V +4 cycles, 100ns per level @ 40 V	1.5+4	Positive	150 µs
ChB	5 level	1.5 cycle, 200 ns per level @±80 V +4 cycles, 100ns per level @ 40 V	1.5+4	Negative	150 µs
ChC	5 level	1.5 cycle, 100 ns per level @±80 V +4 cycles, 100ns per level @ 40 V	1.5+4	Positive	150 µs
ChD	5 level	1.5 cycle, 100 ns per level @±80 V +4 cycles, 100ns per level @ 40 V	1.5+4	Negative	150 µs

Figure 14. Acquisition by program “4”

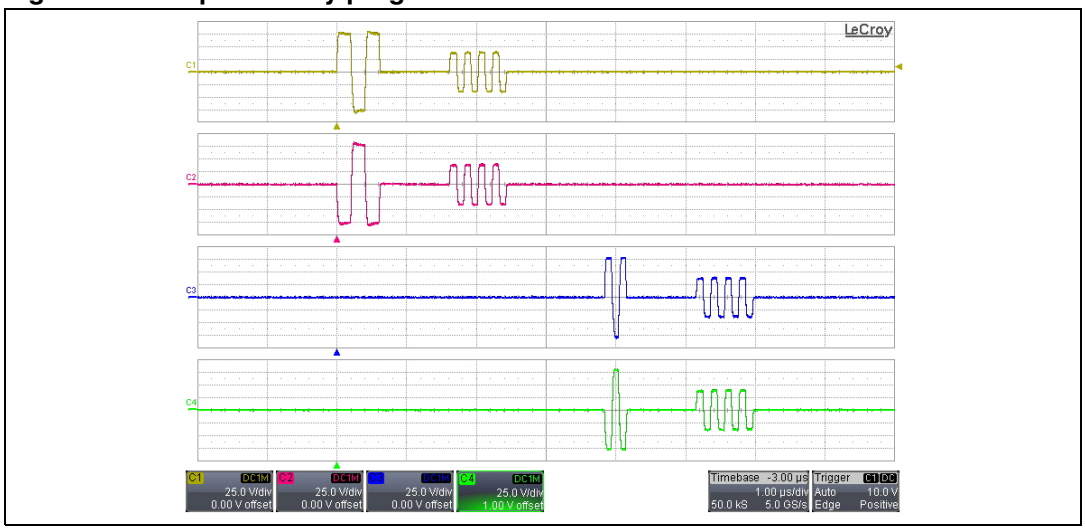

LeCroy
C1
C2
C3
C4
C1 DC1M 25.0 V/div 0.00 V offset
C2 DC1M 25.0 V/div 0.00 V offset
C3 DC1M 25.0 V/div 0.00 V offset
C4 DC1M 25.0 V/div -1.00 V offset
Timebase -3.00 µs 1.00 µs/div 50.0 kS 5.0 GS/s
Trigger C1 DC Auto 10.0 V Edge Positive

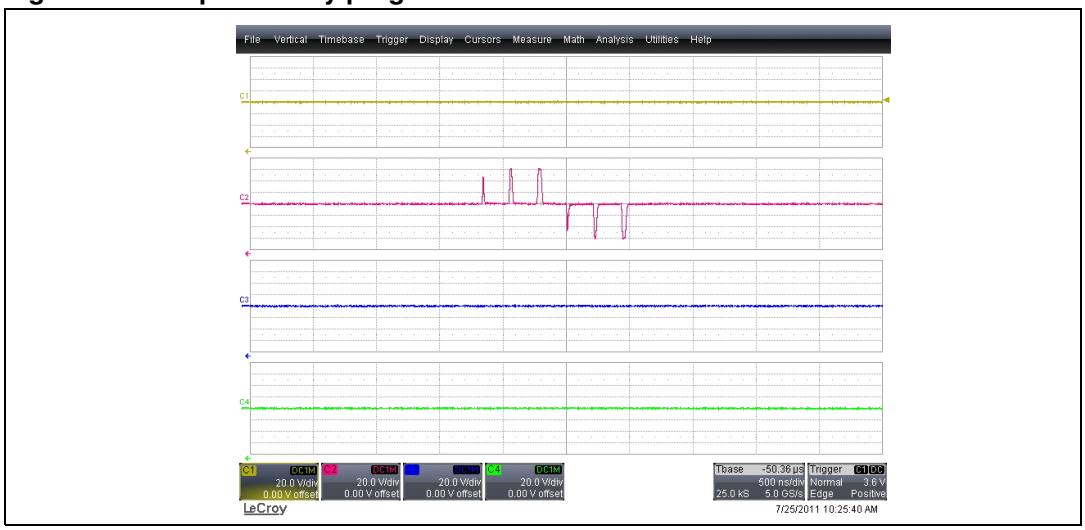
Table 13. Program “5”

Short pulses HV0/1=±60 V; load: 300 pF//100 Ω						
	mode	**Time width pulse**	**Number of pulses**	**Initial pulse**	**H-bridge**	**PRF**
Ch A	SP	10 ns 20 ns 30 ns	6 (3 pos and 3 neg)	Positive	TX0	100 µs
Ch B	SP	10 ns 20 ns 30 ns	6 (3 pos and 3 neg)	Positive	TX0 & TX1	100 µs
Ch C	SP	10 ns 20 ns 30 ns	6 (3 neg and 3 pos)	Negative	TX0	100 µs
CHD	SP to zero	10 ns 20 ns 30 ns	Clamp to 0	Positive	TX0	100 µs

Figure 15. Acquisition by program “5” CHA/C/D

File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help
C1
C2
C3
C4
C1 DC1M 20.0 V/div 0.00 V offset
C2 DC1M 20.0 V/div 0.00 V offset
C3 DC1M 20.0 V/div 0.00 V offset
C4 DC1M 20.0 V/div 0.00 V offset
Timebase -2.19 µs 500 ns/div 25.0 kS 5.0 GS/s
Trigger C1 DC Normal 3.6 V Edge Positive
LeCroy
7/25/2011 10:24:35 AM

Figure 16. Acquisition by program “5” CHB


File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help
C1
C2
C3
C4
C1 DC1M 20.0 V/div 0.00 V offset
C2 DC1M 20.0 V/div 0.00 V offset
C3 DC1M 20.0 V/div 0.00 V offset
C4 DC1M 20.0 V/div 0.00 V offset
Tbase -50.36 us 500 ns/div 25.0 kS 5.0 GS/s
Trigger C1 DC Normal 3.6 V Edge Positive
LeCroy
7/25/2011 10:25:40 AM

A customized pattern can be uploaded by the user into remaining memory slots (through the .dfu file - see user manual UM1083), where it can be tailored to meet the test necessities of the final application.

3.5 STHV748 stage

The STHV748 high-voltage, high-speed pulser generator features four independent channels. It is designed for medical ultrasound applications, but can also be used for other piezoelectric, capacitive, or MEMS transducers.

The device contains a controller logic interface circuit, level translators, MOSFET gate drivers, noise blocking diodes, and high-power P-channel and N-channel MOSFETs as output stages for each channel. There is also clamping-to-ground circuitry, anti-leakage, an anti-memory effect block, a thermal sensor, and a HV receiver switch (HVR_SW), which guarantees a strong decoupling during the transmission phase.

Moreover, the STHV748 includes self-biasing and thermal shutdown blocks (see block diagram in *Figure 17*). Each channel can support up to five active output levels with two half bridges. The output stage of each channel is able to provide ±2 A peak output current. In order to reduce power dissipation during continuous wave mode, the peak current is limited to 0.6 A (a dedicated half bridge is used).

Note: For further information, please refer to the STHV748 datasheet.

The STEVAL-IME003V1 permits the user to configure the special pins of the STHV748 (see *Table 14*). In order to clarify the use and the functionality of these pins, a short explanation is provided below:

- INT_BIAS allows the minimizing of the power consumption. If INT_BIAS=0, the self-voltage reference is not supplied. By supplying the reference externally, the total power consumption is reduced.
- THSD is a thermal flag. The output stage of the THSD pin is an NMOS channel open-drain, so it is necessary to connect the external pull-up resistance (R58, 10 kΩ) to the positive low-voltage supply (see *Figure 17*). If the internal temperature surpasses 160 °C, THSD goes down and puts all the channels into HZ state. By

externally forcing THSD to a positive low-voltage supply, the thermal protection is disabled.

– D_CTR can be used to optimize 2nd HD performance by tuning the fall propagation delay (TDF - see the datasheet for the STHV748 for further details). If D_CTR is equal to ground, TDF has the nominal value. If D_CTR is being varied from 2 V to 4.2 V, TDF can be changed from -1 ns to +600 ps, with respect to the nominal value.

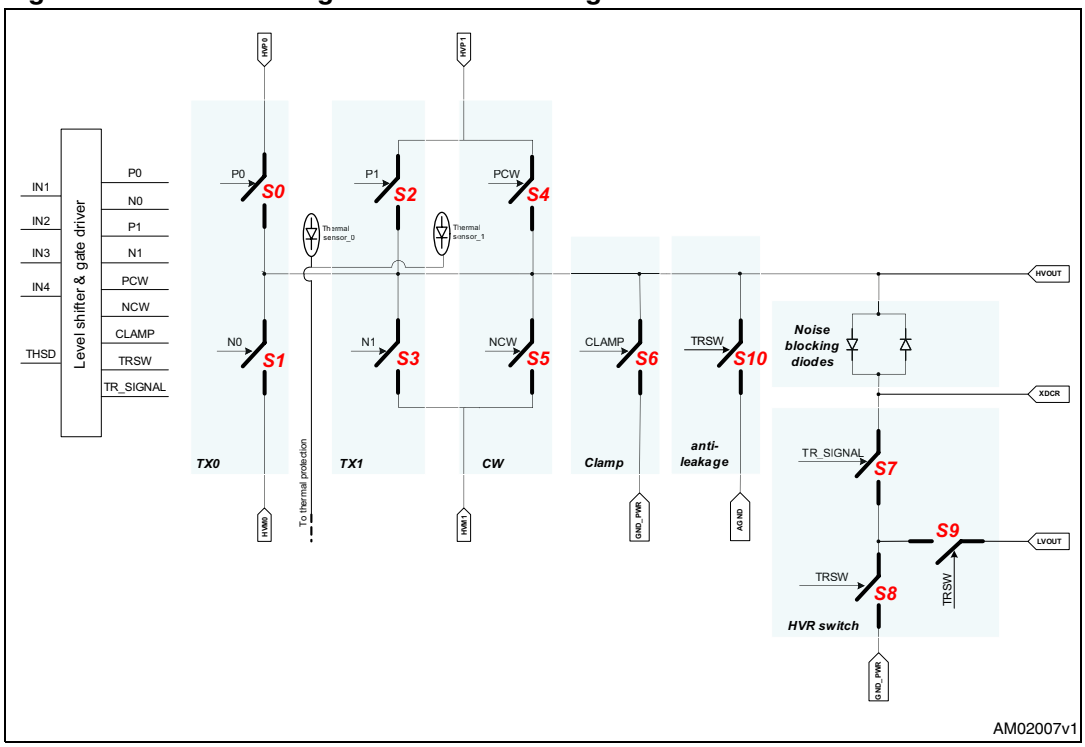
– EXPOSED-PAD is internally connected to the substrate. It can be floating or connected to a 100 V capacitance toward ground, in order to reduce noise during the receiving phase.

The fixed configuration of these pins is described *Table 14*.

Table 14. STHV748 special pin configuration

Special pins on the PCB demo		
Name	**Description**	**Status on board**
INT_BIAS (pin 64)	With INT_BIAS=1, the IC internally generates the reference voltages on REF_HVP1/0 (pin 7, 10, 39, 42) and REF_HVM1/0 (pin 2, 15, 34, 47). These voltages are set VDDP below HVP and VDDP above HVM, respectively: REF_HVM# = HVM# + VDDP REF_HVP# = HVP# - VDDP When INT_BIAS=0, it is required that an external voltage is applied to REF_HVM# and REF_HVP# pins	Active – forced to 3 V through R57=10 kΩ
THSD (pin 32)	Thermal shutdown pin	Active (J24 closed between 1 to 2 – forced to 3 V through R58=10 kΩ). The user can monitor the THSD status on TP3 (test point). Moreover, the user can give the control to FPGA by shorting J24 between 2 and 3
D_CTR (pin 16)	Delay control pin	Not active – forced directly to ground
EXPOSED-PAD	Substrate	Not active – connected to ground through C82=0.22 µF

Figure 17. STHV748 single channel block diagram



The STHV748 output waveforms can be displayed directly for each channel Ch A/B/C/D using an oscilloscope by connecting the scope probe to the J22, J23, J25, and J26 BNC connectors. Also, the user can select whether or not to connect the on-board equivalent load, a 270 pF 200 V capacitor paralleled with a 100 Ω, 2 W resistor (through J20, J21, J27, J28). A coaxial cable can also be used to easily connect the user transducer. Additionally, four more low voltage outputs are available to receive the echo traduced signal coming from the piezo-element through HVR_SW (J16, J17, J29, J30).

The main issues in this PCB design are the capacitance values, to ensure good filtering and an effective decoupling between the low voltage inputs (IN1, IN2, IN3, IN4, and EN for each channel) and the HV switching signals (XDCR, HVOUT, etc.,) which is ensured by the layer separation used.

3.6 Operating supply conditions

Table 15. DC working supply conditions

Operating supply voltages					
Symbol	**Parameter**	**Min**	**Typ.**	**Max**	**Value**
VDDP	Positive supply voltage	2.7	3	3.6	V
VDDM	Negative supply voltage	-2.7	-3	-3.6	V
VDD	Positive logic voltage	2.4	3	Min(3.6,VDDP+0.3)	V
HVP0	TX0 high voltage positive supply			95	V
HVP1	TX1 high voltage positive supply			95	V

Table 15. DC working supply conditions (continued)

Operating supply voltages					
Symbol	**Parameter**	**Min**	**Typ.**	**Max**	**Value**
HVM0	TX0 high voltage negative supply	-95			V
HVM1	TX1 high voltage negative supply	-95			V

Note: The high voltage pins must be HVP0 ≥ HVP1 and HVM1 ≥ HVM0

Table 16. Current consumption in CW mode, @ 5 MHz, HVP/M1

Current consumption			
Symbol	**Parameter**		**Value**
IVDDP	Positive supply current	8.6	mA
IVDDM	Negative supply current	13.5	mA
IDVDD	Positive logic current	0.11	mA
IHVP1	TX1 high voltage positive supply current	14.5	mA
IHVM1	TX1 high voltage negative supply current	11	mA

4 Connectors

4.1 Power supply

The STEVAL-IME003V1 board has to be powered by the J4, J1, J2 and J3 connectors shown in the illustrations below.

Figure 18. Power supply connector J4

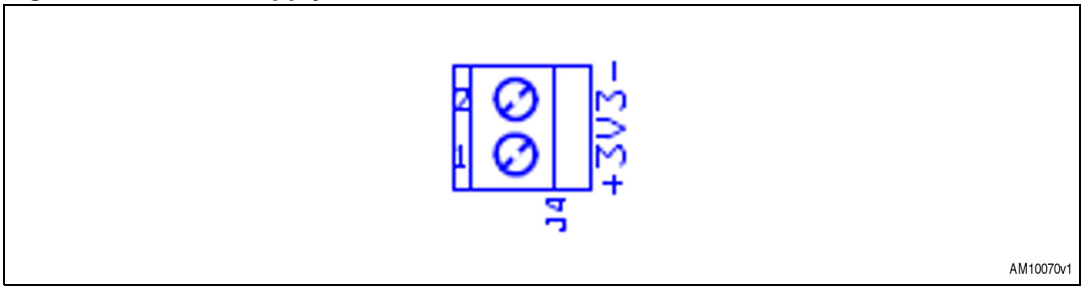


Figure 19. Power supply connector J1

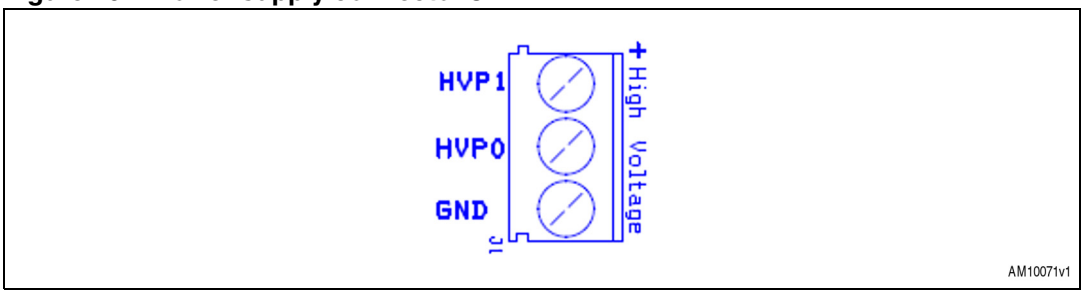


Figure 20. Power supply connector J2

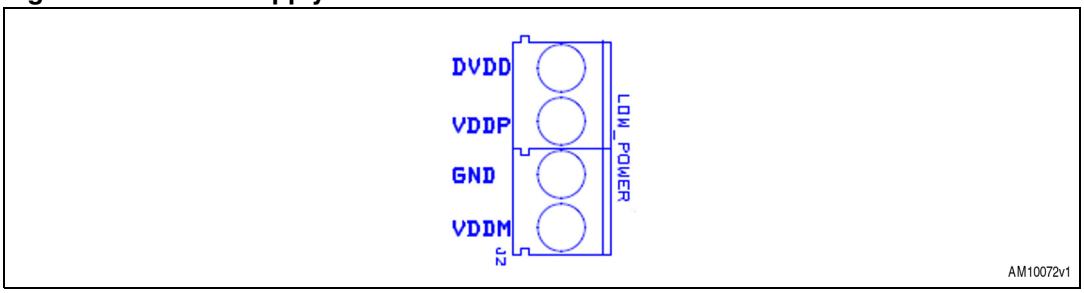
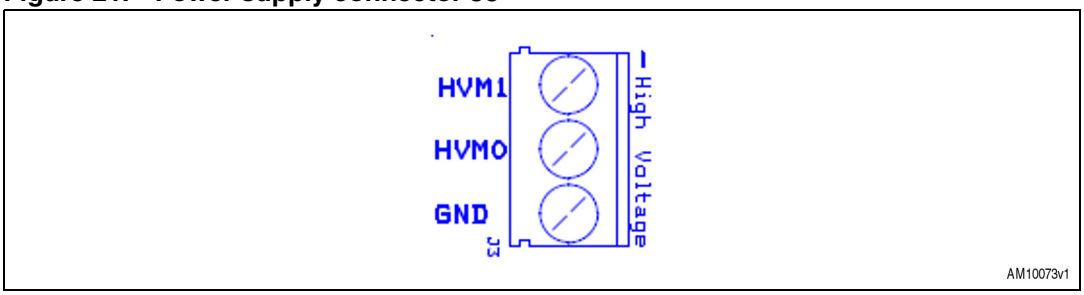


Figure 21. Power supply connector J3



The correct power-up sequence is:

1. VDDP
2. VDDM or VDD
3. VDD or VDDM
4. HVM0
5. HVP0
6. HVM1 or HVP1
7. HVP1 or HVM1

4.2 MCU

Figure 22. USB mini-B connector (CN1)

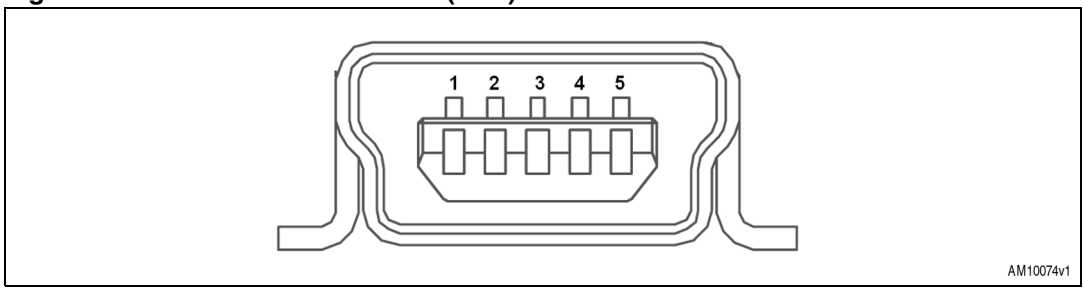


Table 17. USB Mini B connector pinout

PIN number	Description
1	Vbus (power)
2	DM (STM32 PA11)
3	DP (STM32 PA12)
4	N.C.
5	Ground

Figure 23. SWD (J40)

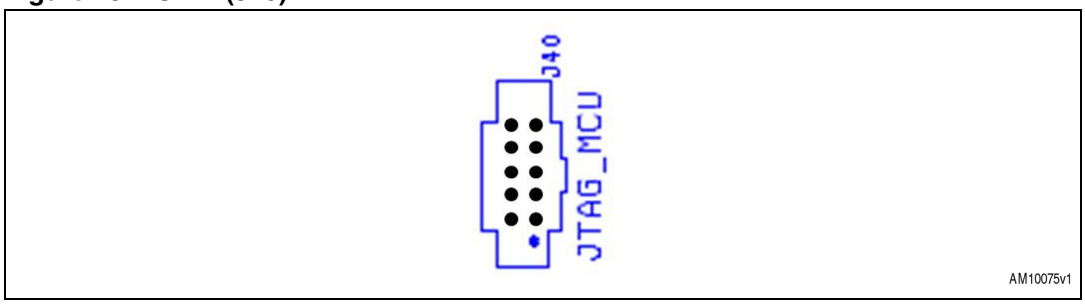


Table 18. JTAG/SWD connector pinout

PIN number	Description
1	MCU_3V3
2	JTMS
3	GND
4	JTCK
5	GND
6	JTDO
7	GND
8	JTDI
9	GND
10	RESET#

4.3 SPI Flash memory

Figure 24. Memory expansion connector (J10)

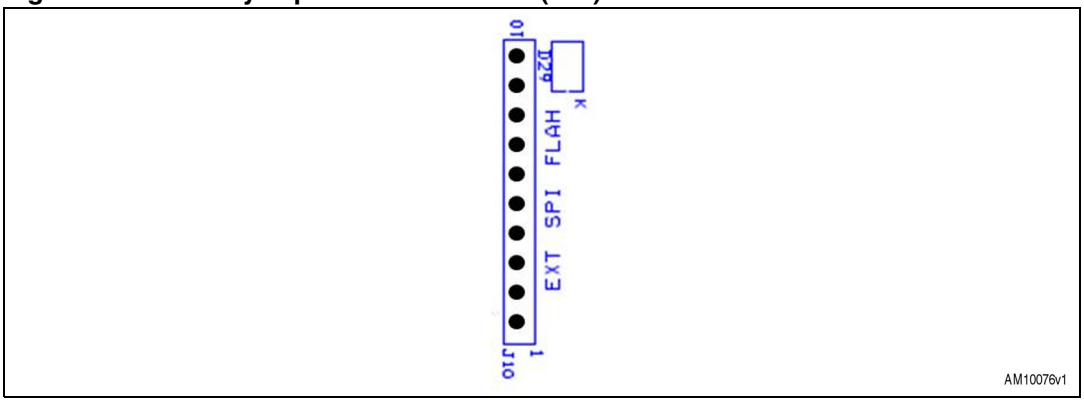


Table 19. Memory expansion connector pinout

PIN number	Description
1	MCU_FPGA_PROG (not used)
2	SPI MISO3
3	SPI MISO2
4	SPI CS
5	SPI MOSI
6	SPI MISO
7	SPI CLK
8	GND

Table 19. Memory expansion connector pinout (continued)

PIN number	Description
9	3.3V
10	CHECK

Note: This memory is mutually exclusive with on-board Flash memory; unfit J38 before plugging in expansion memory over J10. The relevant LED (D29) will turn on.

4.4 FPGA

Figure 25. STHV748 I/O connector (J6) not mounted on the board

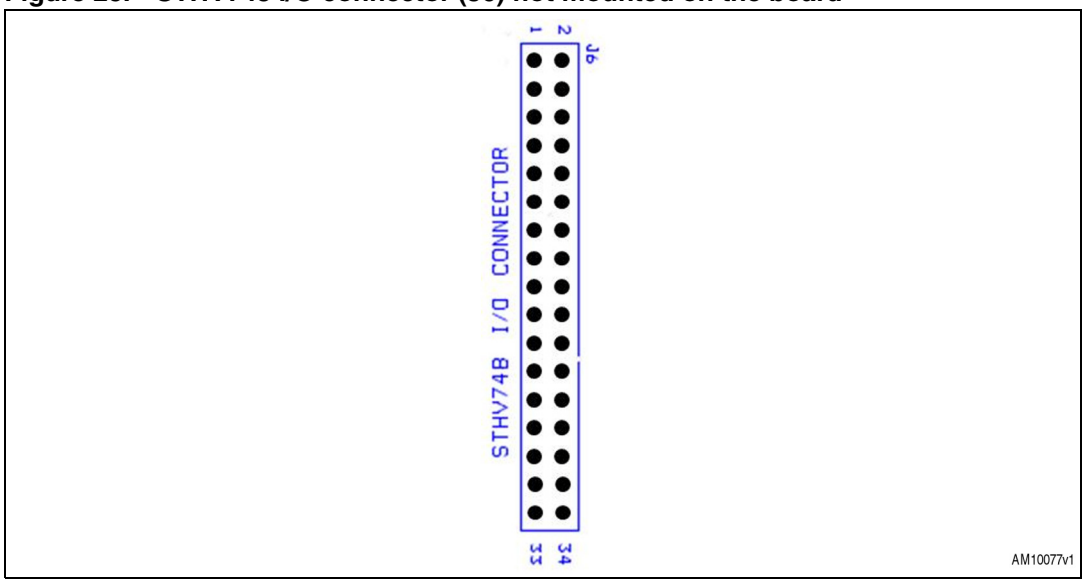


Table 20. STHV748 I/O connector pinout

PIN number	Description (STHV748 pin)	PIN number	Description (STHV748 pin)
1	DATAOUT9 (IN1D)	2	GND
3	DATAOUT13	4	GND
5	DATAOUT10 (IN2D)	6	GND
7	DATAOUT14	8	GND
9	DATAOUT6 (IN1C)	10	GND
11	DATAOUT15	12	GND
f13	DATAOUT7 (IN2C)	14	DATAOUT2 (IN3A)
15	DATAOUT8 (IN3C)	16	GND
17	DATAOUT5 (IN3B)	18	GND
19	DATAOUT11 (IN3D)	20	GND
21	THSD_EN	22	GND

Table 20. STHV748 I/O connector pinout (continued)

PIN number	Description (STHV748 pin)	PIN number	Description (STHV748 pin)
23	DATAOUT4 (IN2B)	24	GND
25	3.3V	26	DATAOUT12 (IN4)
27	CLKOUT	28	3.3 V
29	TRIGGEROUT	30	GND
31	DATAOUT0 (IN1A)	32	GND
33	DATAOUT1 (IN2A)	34	DATAOUT3 (IN1B)

5 Schematics

Figure 26. STEVAL-IME003V1 hierarchical blocks

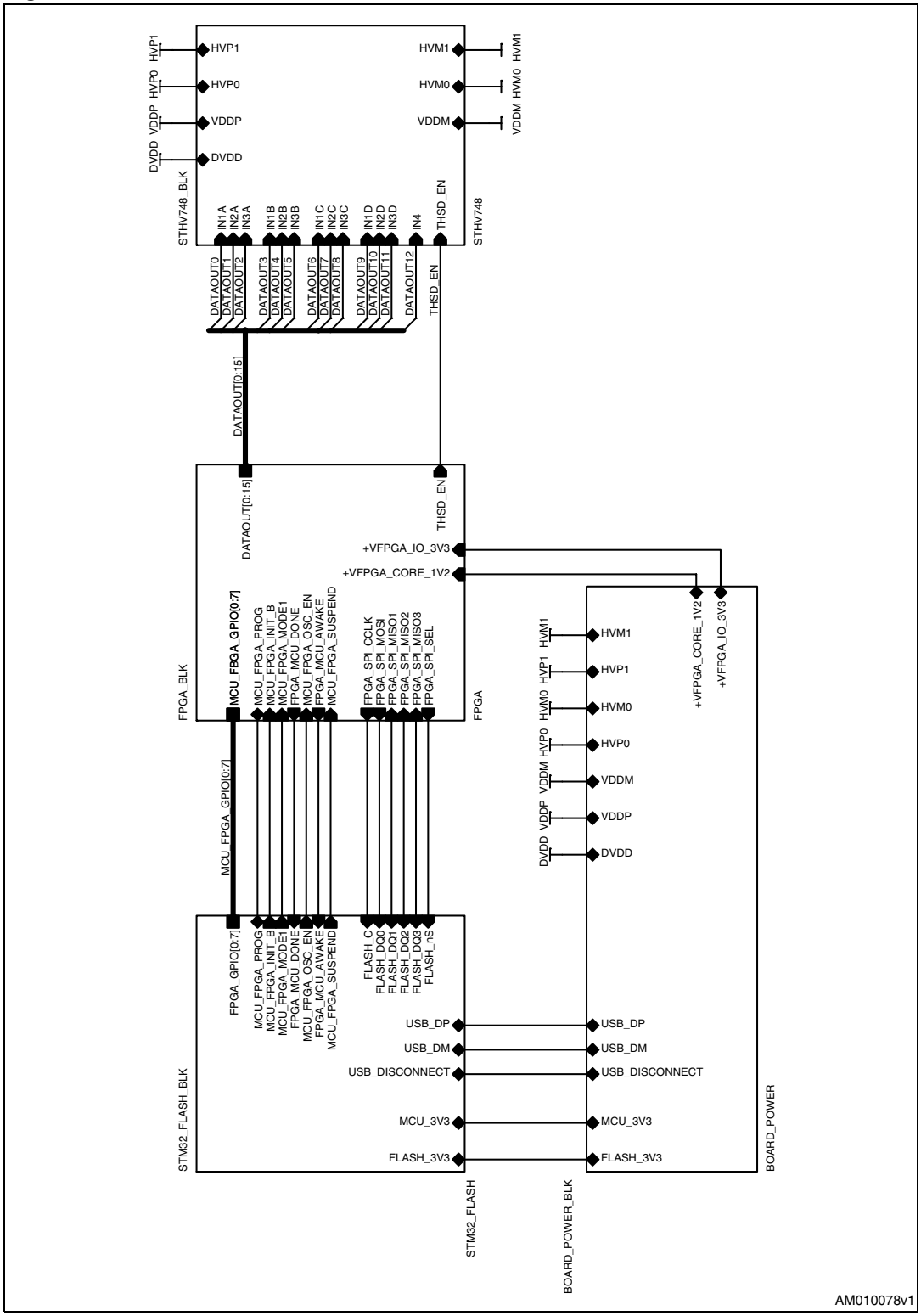


Figure 27. STEVAL-IME003V1 FPGA bank 0 configuration

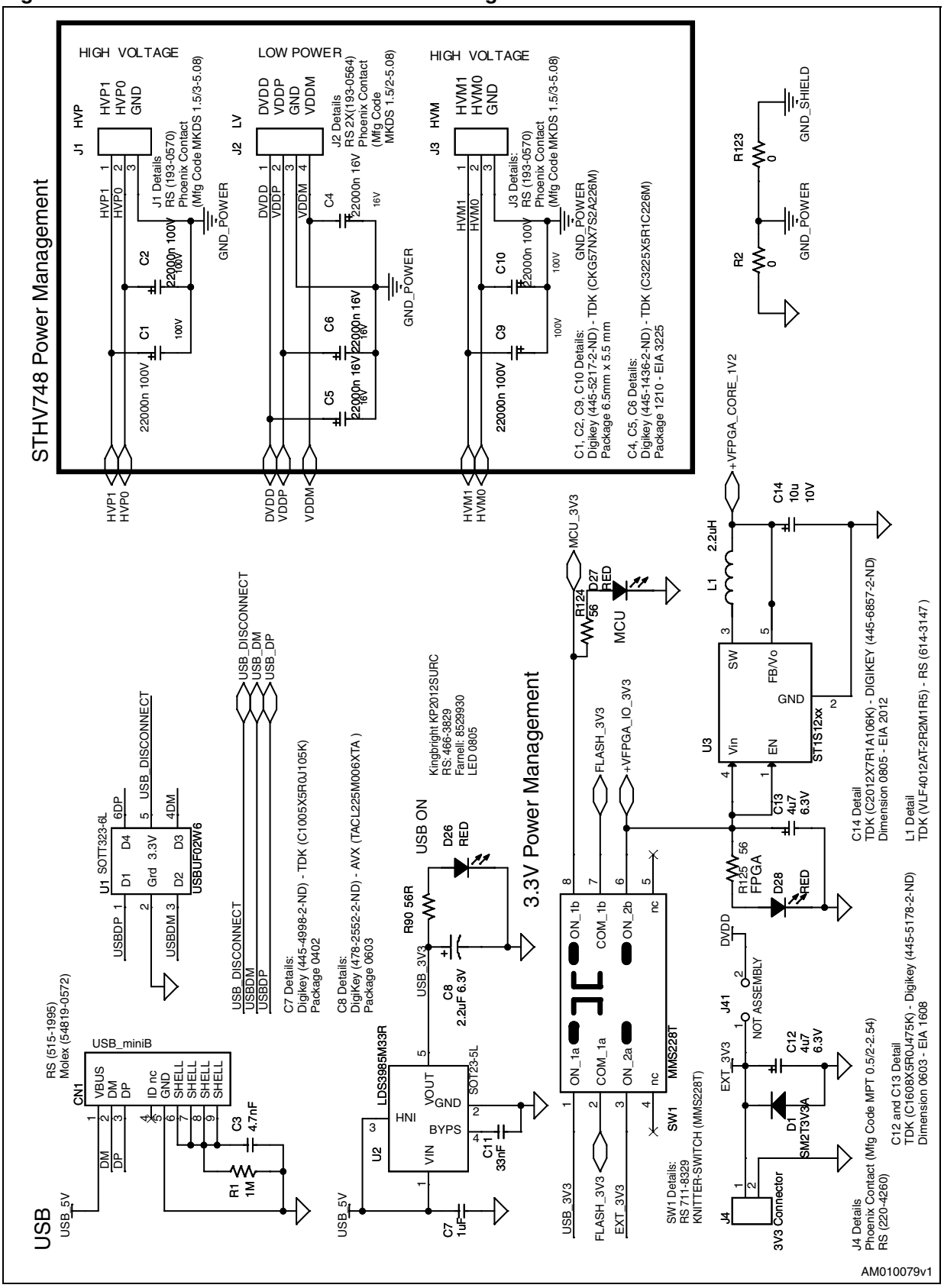


Figure 28. STEVAL-IME003V1 FPGA bank 1 configuration

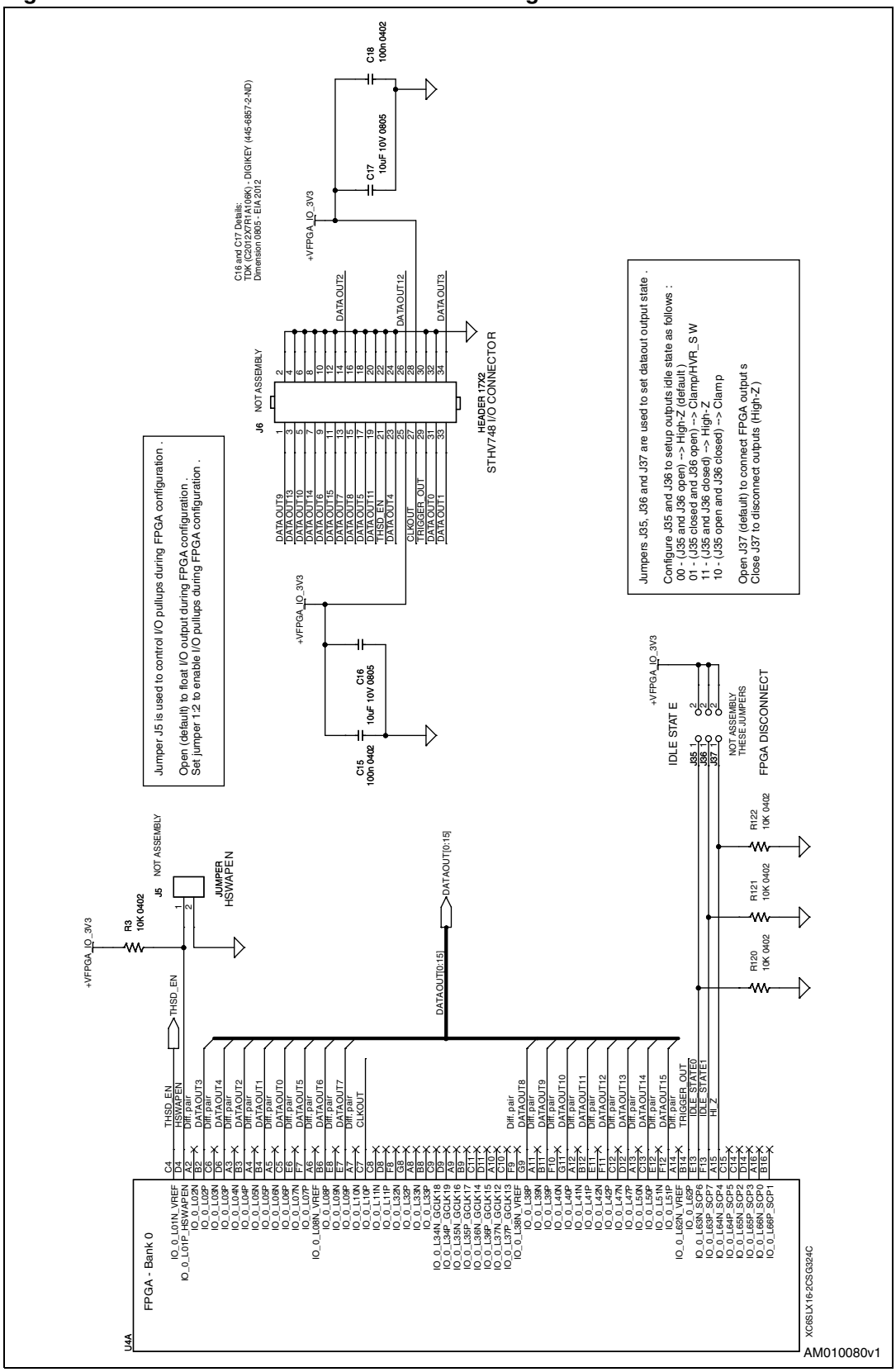

FPGA - Bank 0
U4A
XC6SLX16-2CSG324C
AM010080v1
Jumper J5 is used to control I/O pullups during FPGA configuration .
Open (default) to float I/O output during FPGA configuration .
Set jumper 1-2 to enable I/O pullups during FPGA configuration .
Jumpers J35, J36 and J37 are used to set dataout output state .
Configure J35 and J36 to setup outputs idle state as follows :
00 - (J35 and J36 open) --> High-Z (default)
01 - (J35 closed and J36 open) --> Clamp/HVR_S W
11 - (J35 and J36 closed) --> High-Z
10 - (J35 open and J36 closed) --> Clamp
Open J37 (default) to connect FPGA output s
Close J37 to disconnect outputs (High-Z)
C16 and C17 Details:
TDK (C2012X7R1A106K) - DIGIKEY (445-6857-2-ND)
Dimension 0805 - EIA 2012
HEADER 17X2
STHV748 I/O CONNECTOR
FPGA DISCONNECT
IDLE STAT E
NOT ASSEMBLY
THESE JUMPERS
JUMPER
HSWAPEN
+VFPGA_IO_3V3
THSD_EN
HSWAPEN
CLKOUT
TRIGGER_OUT
IDLE_STATE0
IDLE_STATE1
HI_Z
DATAOUT[0:15]

Figure 29. STEVAL-IME003V1 FPGA bank 2 configuration

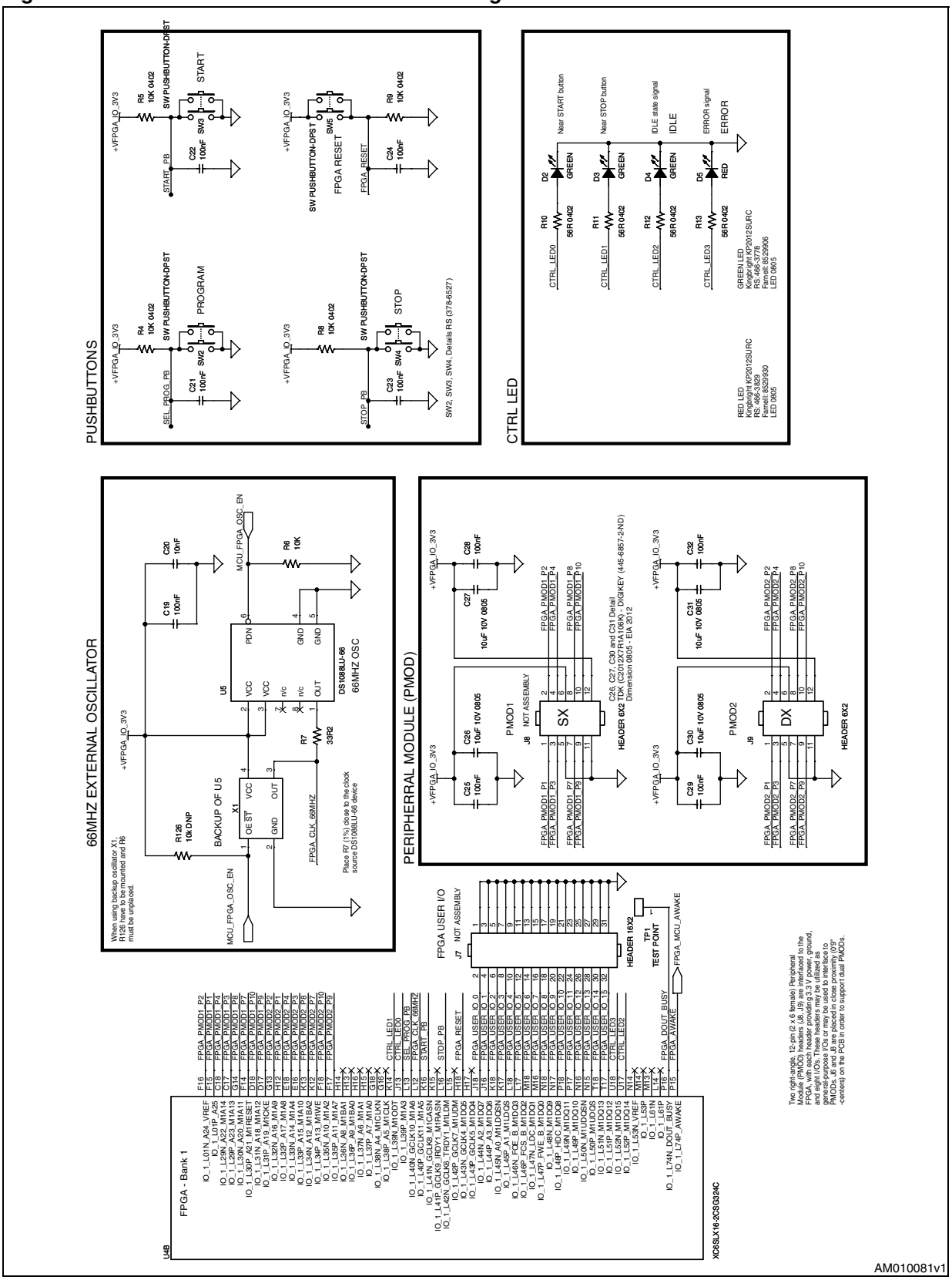


Figure 30. STEVAL-IME003V1 FPGA bank 3 configuration

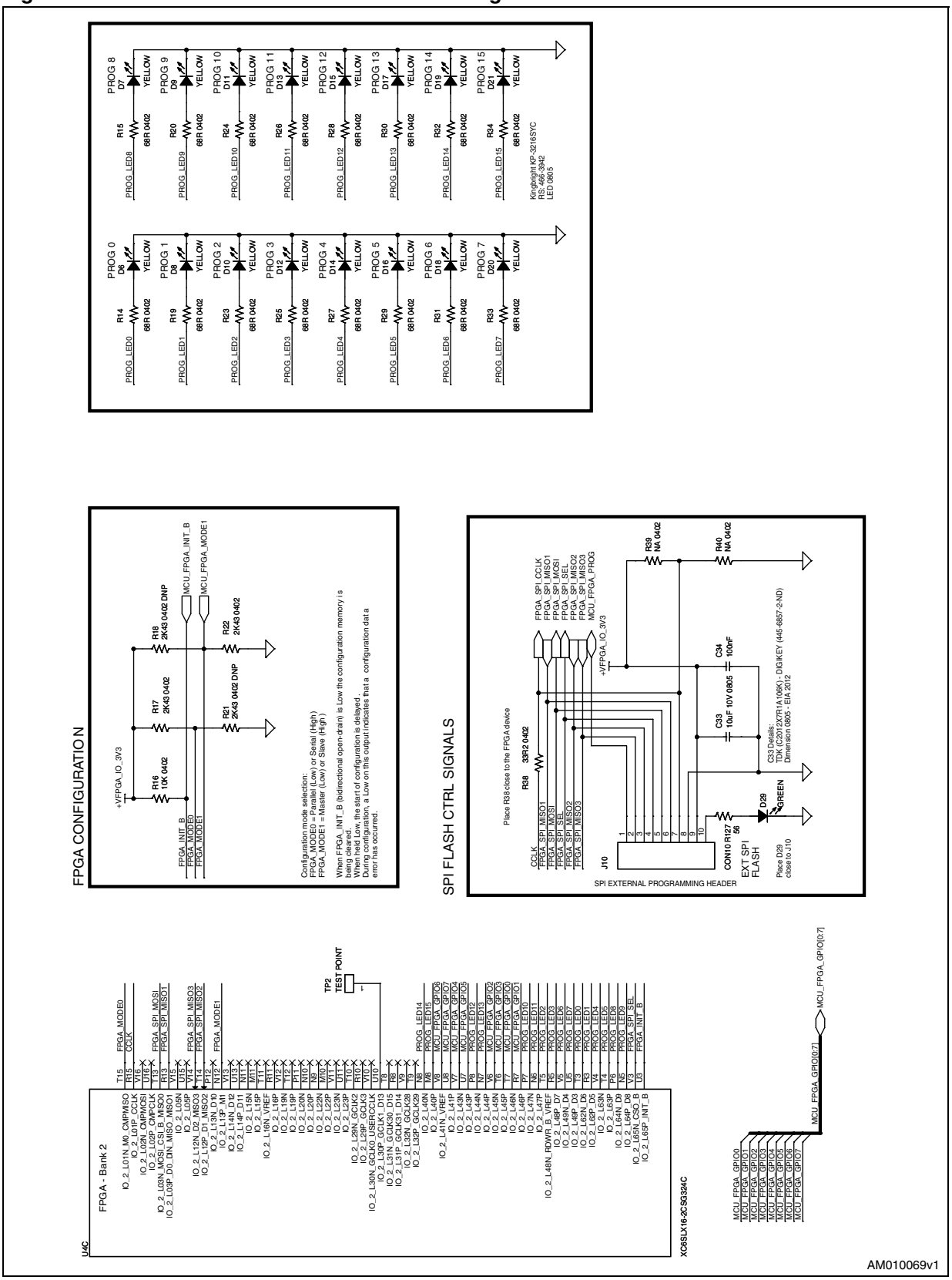


Figure 31. STEVAL-IME003V1 FPGA bank 3 configuration

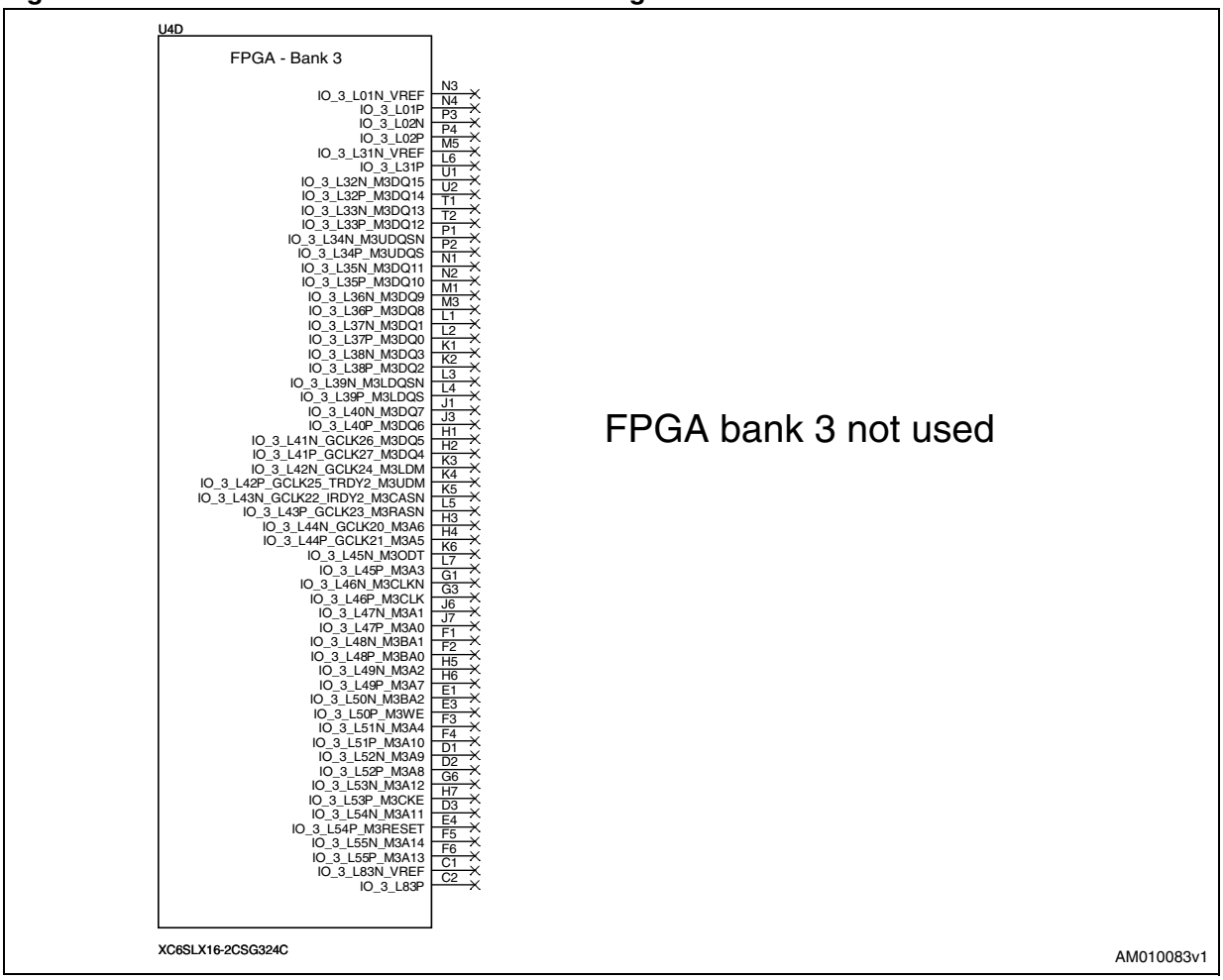


Figure 32. STEVAL-IME003V1 FPGA power and configuration

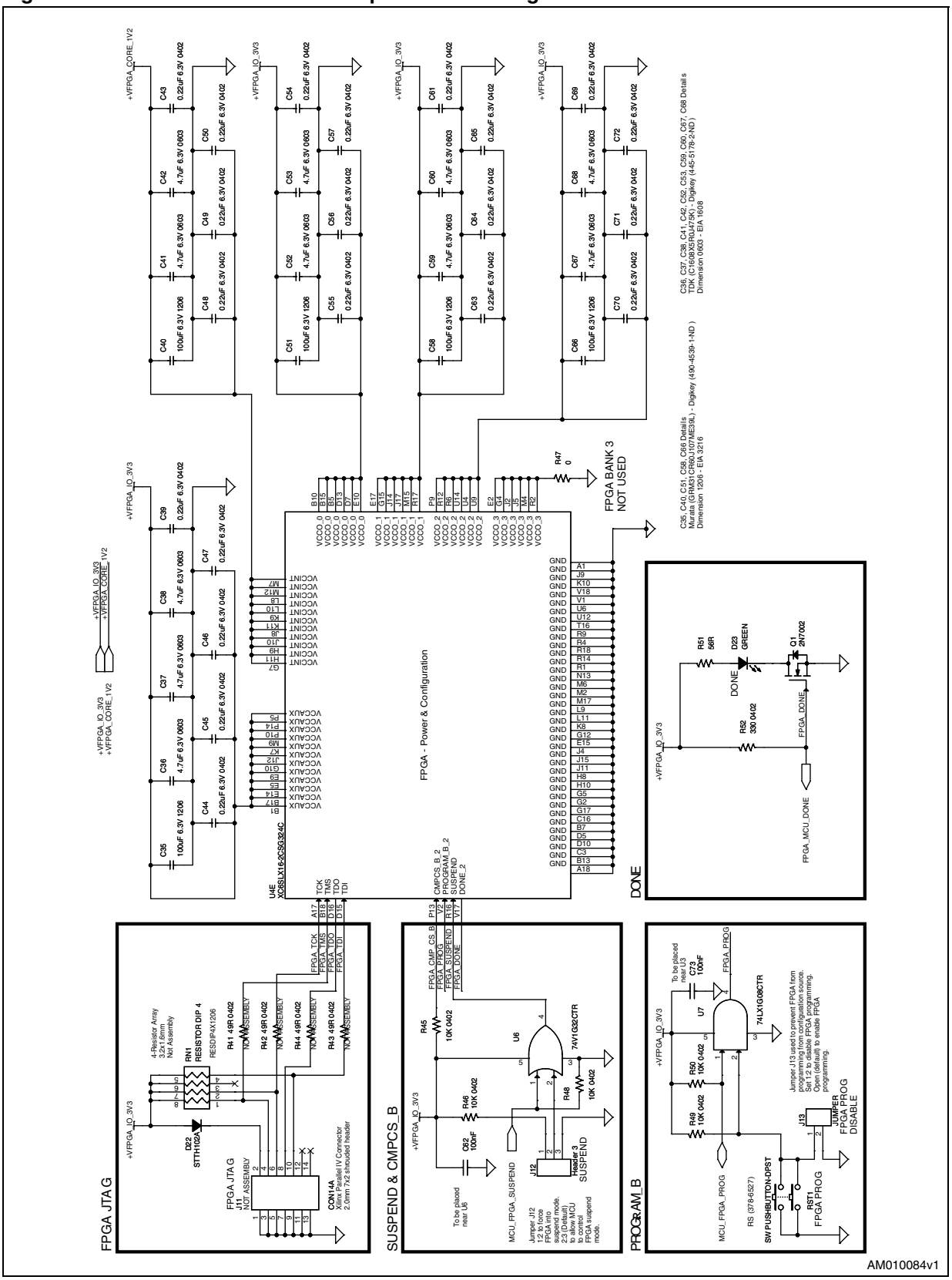


Figure 33. STEVAL-IME003V1 STHV748 configuration

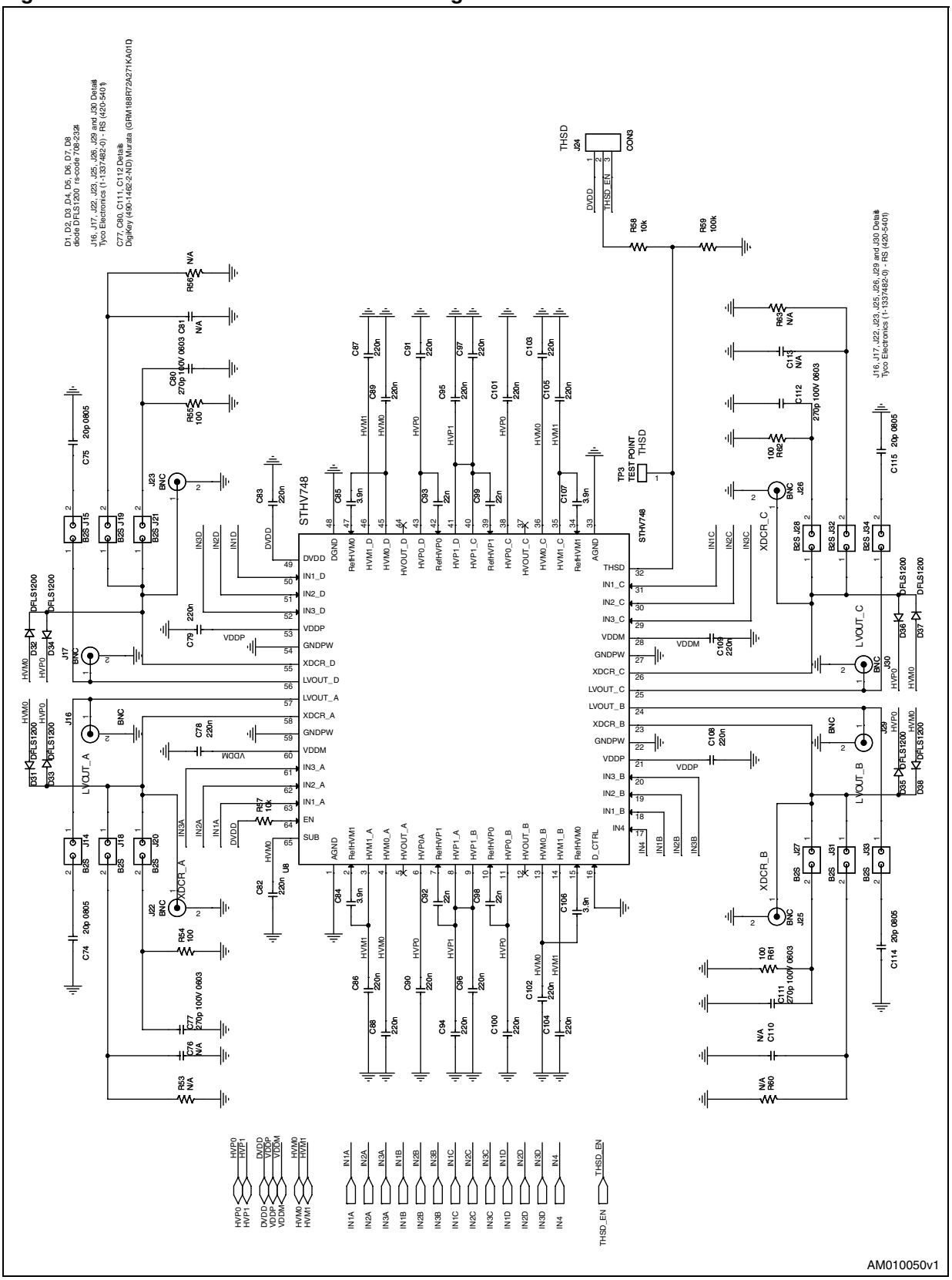
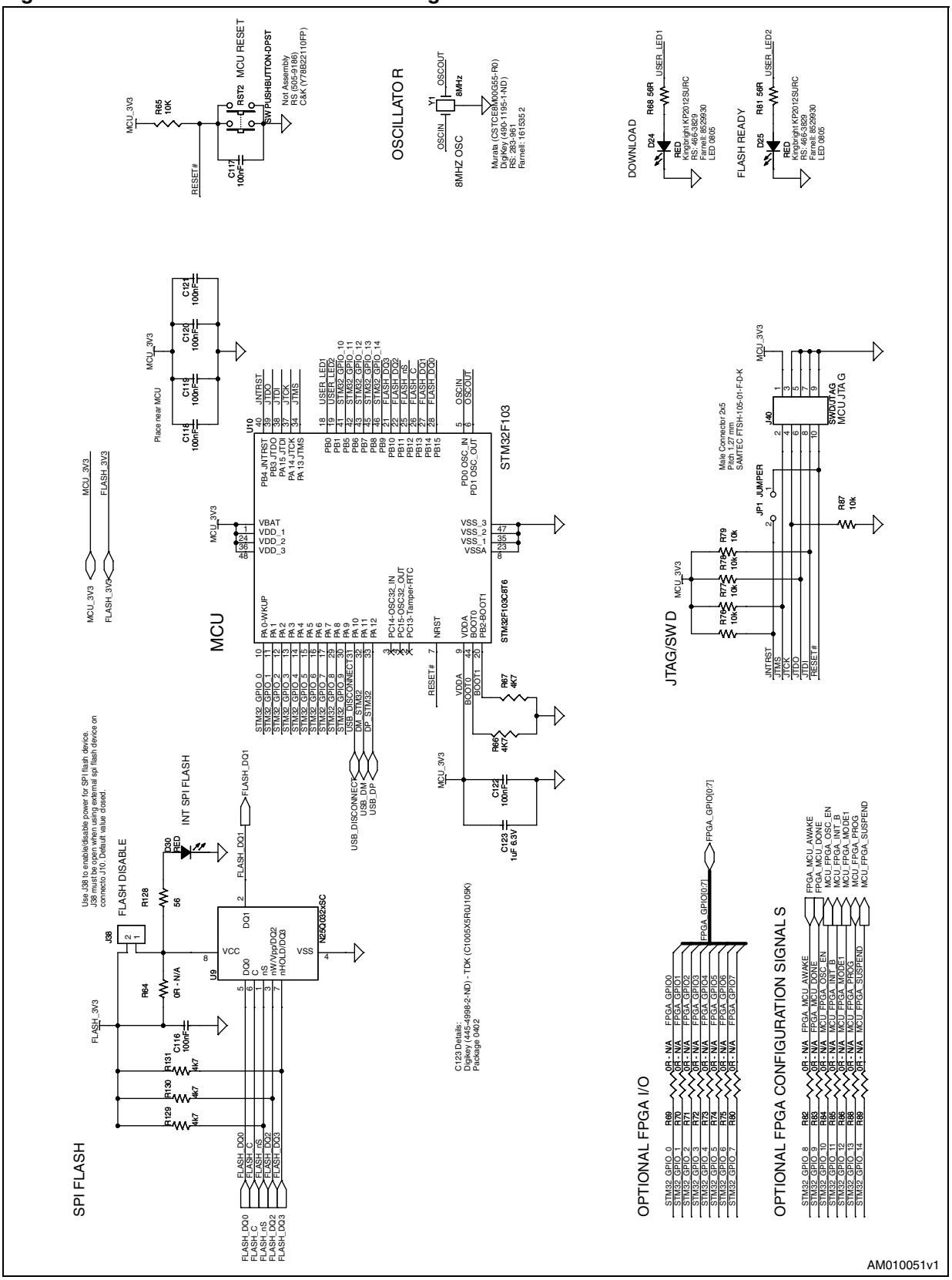


Figure 34. STEVAL-IME003V1 STM32 configuration



6 Revision history

Table 21. Document revision history

Date	Revision	Changes
18-Aug-2011	1	Initial release.
17-Jan-2012	2	– Modified: *Figure 14* and *16* – Modified pattern sequences related to Program "4"

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